TranSwitch®

M13X Device
DS3/DS1 MUX/DEMUX, Enhanced Features
TXC-03305

DATA SHEET

FEATURES

- Multiplexes/demultiplexes 28 DS1 signals to/from a DS3 signal
- Integrated dejitter buffers to GR-499-CORE for all receive DS1 outputs, with bypass option
- M13 or C-bit parity format mode operation
- FEBE, C, or P-bit parity error insertion capability
- DS3 idle signal generators
- DS1 idle signal (QRS, AIS or ESF) generators
- DS3 LOS, LOF, P-bit parity, C-bit parity, AIS and idle detectors
- Integrated PMDL controller
- Receive or transmit DS1 LOS detectors
- DS2 LOF detectors
- External interface for receiving 14 C-bits and transmitting either 13 or 14 C-bits based on a control bit setting
- DS3 and DS2 X-bit access
- DS3 transmit and receive selectable AIS generation and detection
- Supports Intel, Motorola, or multiplexed microprocessor interfaces, and includes interrupt capability
- DS2 transmit/receive X-bit control/status
- 8 or 16-bit wide performance counters
- Reset lead
- Test Access Port for boundary scan
- Single +5V, ±5% power supply
- 208-lead Small Outline Plastic BGA package or 208-lead PQFP package (for M13E replacement)

DESCRIPTION

The M13X CMOS VLSI device provides the functions needed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. It includes some enhanced features relative to the M13E device. A lead (M13X) is provided for selecting functional and software backwards compatibility with the M13E device (TXC-03303). The M13X line side signals typically interface with a TranSwitch ART, ARTE or DART device, a DS3LIM-SN module or other DS3 line circuitry. Terminal side signals interface with commercially available DS1 line interface devices or a TranSwitch T1Fx8 device for DS1 framing. The output DS1 signals can optionally be dejittered via integrated dejitter buffers (DJBs). The DJBs meet and exceed the requirements specified in GR-499-CORE, 1998.

The M13X provides an external transmit (13 or 14 bits) and receive (14 bits) interface for the 21 C-bits while operating in the C-bit parity mode. The FEAC channel (C3) can be accessed via the external interface or the M13X memory. An integrated PMDL controller is provided for transmitting and receiving HDLC encapsulated PMDL messages. Buffering of PMDL messages is provided in the transmit and receive directions. Message lengths of arbitrary size can be transmitted or received. The M13X memory map contains up to 64 8-bit register locations for software control, performance counters, and alarm reporting. The microprocessor interface provides for connection to an Intel or Motorola-compatible microprocessor, or for use of a multiplexed address/data bus. An interrupt lead with programmable polarity is provided.

APPLICATIONS

- Single-board M13 multiplexer
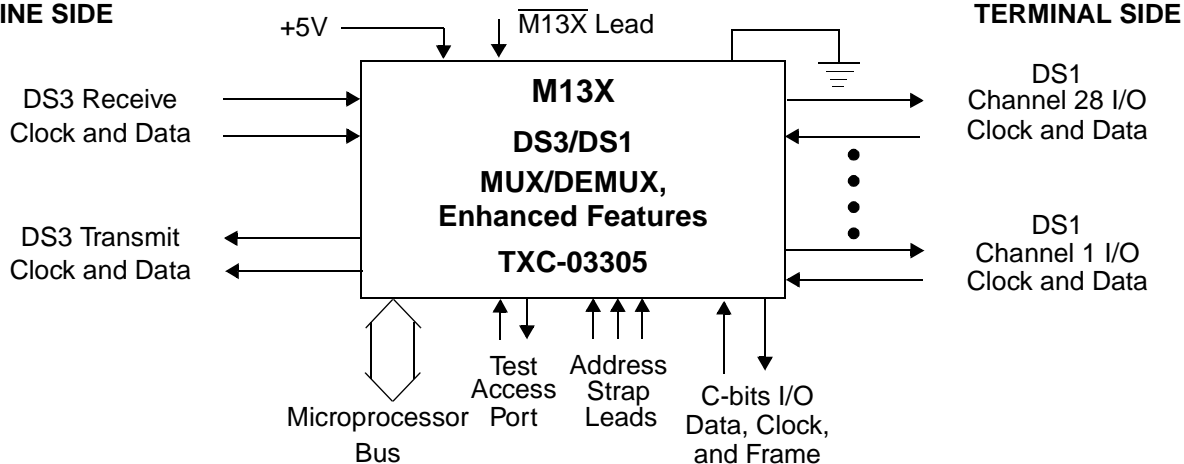- Compact add/drop mux
- Fractional T3
- Channelized T3

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* Please note that TranSwitch provides documentation for all of its products. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

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BLOCK DIAGRAM

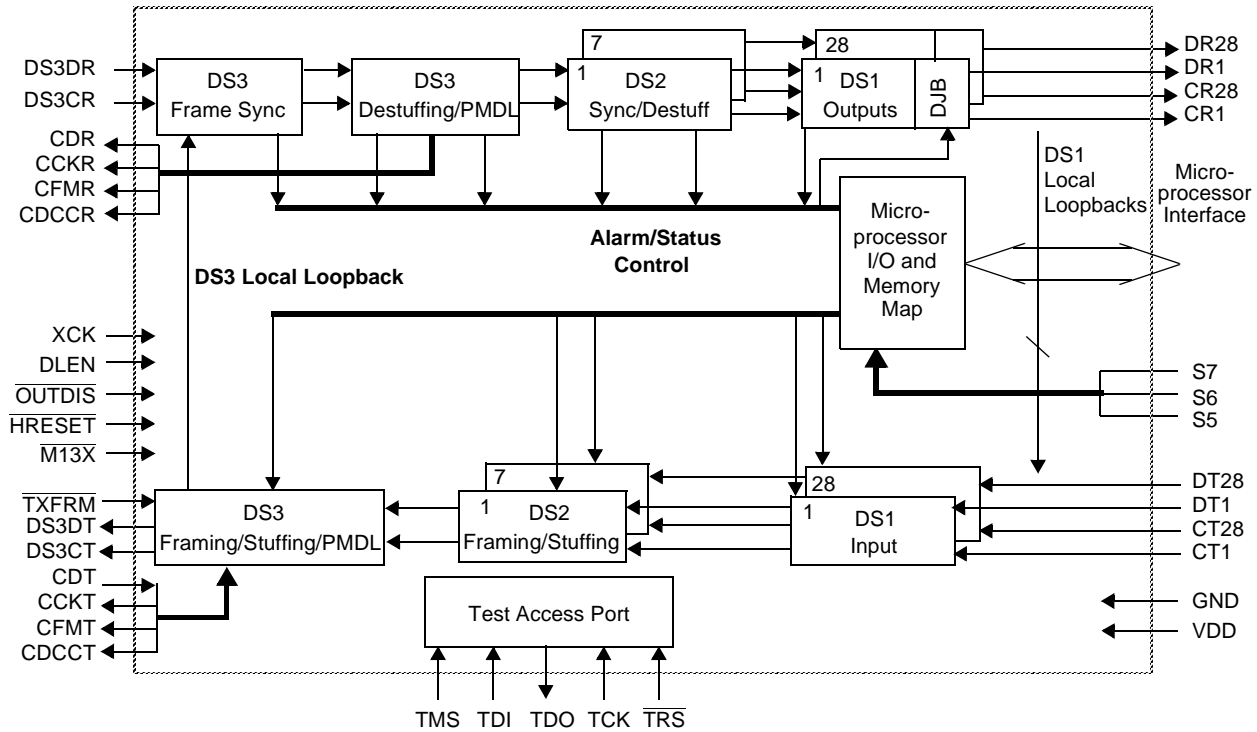A block diagram for the M13X device is shown in Figure 1 below.

Figure 1. M13X TXC-03305 Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 shows a simplified block diagram of the M13X and its signal leads. The M13X is packaged in a 208-lead small outline Plastic Ball Grid Array (PBGA) package or a 208-lead Plastic Quad Flat Package (PQFP). The PQFP version is intended to be used as a replacement for TranSwitch's M13E device (TXC-03303-AIPQ) and is not recommended for new designs. The PBGA version is intended for new designs.

The M13X in the PBGA or PQFP packages, with the exception of the boundary scan, can be configured to be functionally compatible with, and have the same memory map as, the M13E device, by applying a high to the $\overline{\text{M13X}}$ lead. The enhanced features included in the M13X can be enabled by applying a low to the $\overline{\text{M13X}}$ lead. These enhanced M13X features are:

- Transmit/receive PMDL (Path Maintenance Data Link) controller
- Interrupt request lead with programmable polarity and associated interrupt mask bits
- Integrated dejitter buffer (DJB) on all receive DS1 outputs with optional bypass capability
- 16-bit performance counters.
- NEW bit in register 1DH does not become set to one again after it is cleared when a constant FEAC message is received.

When the $\overline{\text{M13X}}$ lead is set to high, the M13X enhanced features listed above are disabled and cannot be accessed.

In the receive direction, DS3 data (DS3DR) is clocked into the M13X on rising edges of the DS3 input clock (DS3CR). The data and clock signals may be derived from any line interface unit such as TranSwitch's ART, ARTE, DART or DS3LIM-SN, or from other line circuitry.

The DS3 Frame Sync block searches for and locks to the DS3 frame, as specified in Bellcore GR-499-CORE "Transport System Generic Requirements," and in ANSI T1.107-1995. The M13X receiver monitors the DS3 signal for out of frame, loss of signal, a DS3 AIS, DS3 idle signal, P-bit parity, the state of the X-bits, and loss of clock. The DS3 AIS detection mechanism is software selectable, with a choice of six detectors. These range from full compliance to T1.107-1995 to unframed all ones AIS detection. Control bits are also provided in memory which allow all, some of, or none of the DS3 alarms to cause the insertion of AIS into the receive DS1 channels.

In the M13 format mode, destuffing from DS3 to DS2 is performed based on the states of the C-bits in the DS3 subframes. If two or three of the C-bits in a subframe are ones, the associated stuff bit is interpreted as being a stuff bit and is removed from the data stream and discarded.

In the C-bit parity mode, the C-bits are allocated for network performance. The M13X performs Far End Alarm and Control (FEAC) detection, C-bit parity error detection, and Far End Block Error (FEBE) detection. FEAC loopback requests and alarm/status information are provided in the memory map. In addition, the states of 14 C-bits (C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21) are provided at a serial interface (CDR), along with an output clock signal (CCKR), framing pulse (CFMR), and data link indicator pulse (CDCCR). The data link indicator pulse identifies the location of the data link bits, C13, C14, and C15. If the $\overline{\text{M13X}}$ lead is tied low, the receive PMDL (Path Maintenance Data Link) controller can be enabled via a control bit. The receive PMDL controller is used to extract PMDL messages of any length. FCS error detection, ABORT detection, End of Message, Start of Message, Invalid Frame Detected, and receive PMDL FIFO status can be monitored via the microprocessor interface.

The M13X synchronizes and extracts the 28 DS1 channels from the seven DS2 channels. Each of the DS2 channels is monitored for out of frame. The M13X may generate AIS in each of the DS1 signal tributaries corresponding to the DS2 channel(s) that lost frame, depending on the DS1 AIS alarm insertion control bits. DS2 to DS1 destuffing is based on the states of the three C-bits in each DS2 subframe. If two or three of the C-bits in one of the DS2 subframes are ones, the stuff bit for that subframe is discarded. In the M13 format mode, the DS2 C-bits or stuffing bits are used for DS1 remote loopback requests for either the M13 or C-bit Parity format

modes. The M13X provides control bits in the memory map for selecting the remote loopback detection mechanism. The destuffing operation is still active during loopback request and operation. In addition to DS2 synchronization, destuffing, and remote loopback request detection, the M13X also extracts the seven DS2 X-bits and provides them to a register.

An option is provided that allows the received or transmitted DS1 channels to be monitored for loss of signal. Receive data for each of the DS1 channels (DRn) is clocked out of the M13X on rising edges of the associated clock signal (CRn), where n = 1 - 28. In addition, the M13X provides a stable DS1 clock signal for the data signals received during AIS periods. When the $\overline{M13X}$ lead is held low, dejitter buffers (DJBs) can be enabled via a control bit to dejitter the receive DS1 outputs. The DJBs meet and exceed GR-499-CORE specifications.

In the transmit direction, DS1 transmit data (DTn) is clocked into the M13X on rising edges of the clock input (CTn) for each of the 28 DS1 channels. A DS1 Input block, which consists of a FIFO and supporting logic, is provided for each DS1 channel. Under software control, the M13X can invert the transmit data signals, or the clock signals, for all 28 DS1 channels. The data inversion feature provides compatibility with certain T1 line interface devices, while the clock inversion feature allows back-to-back M13X operation.

The DS1 Input block is also used to insert one of three idle patterns from a common generator into a DS1 bit stream, under software control. The selection of the idle pattern is common to all 28 DS1 channels. The idle patterns are: a QRS, an Extended Super Frame DS1 (ESF) format with all ones in DS0 channels 1 through 24, and an AIS format (all ones).

Each DS1 signal is multiplexed into the respective DS2 frame, with the stuff bits inserted based on the fill level of an internal FIFO. When the fill of the FIFO drops below half full, a stuff bit is inserted into the DS1 bit stream in the DS2 signal. The DS2 signal is formed by combining four DS1 signals. In each frame there are 287 data bit positions and one stuff bit per DS1 channel (for a DS1 total of 1152 bits) and 24 overhead bits, for a frame total of 1176 bits. The overhead bits are used for framing, X-bit channel and stuff control.

The DS3 signal is partitioned into M-frames of 4760 bits each. The M-frames are divided into seven M-subframes having 680 bits each. Each M-subframe is further divided into eight blocks of 85 bits each. Each block uses 84 bits for payload and one bit for frame overhead. There are 56 overhead bits in each M-frame: the M-frame alignment uses three bits, the M-subframe alignment (F-bits) uses 28 bits, 21 bits are defined as C-bits, two bits are assigned for parity, and two bits are assigned for the X-bit channel. A frame synch input, $\overline{TXFRM}$, is provided and can optionally be used to align the DS3 overhead bits in the DS3DT output.

The DS3 frame is constructed and timed according to the operating mode, i.e., C-bit parity mode or M13 format mode. In the C-bit parity mode, all seven of the DS2 stuff bits are always fixed as stuff, resulting in 7 pseudo DS2 frames of 671 bits per DS2 frame in each DS3 frame, for a DS2 rate of 6.3062723 Mbit/s. Since stuffing always occurs, the 21 C-bits are assigned for other functions, as shown in Figure 2. A C-bit interface is provided for transmitting 13 or 14 C-bits (C2, C3-depending on the state of bit 7 of register 19H (C3CLKI), C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, C21). The external transmit C-bit interface consists of a serial data input (CDT), an output clock (CCKT), a data link indicator pulse (CDCCT), and an output framing pulse (CFMT). The data link indicator pulse identifies the location of the three data link bits, C13, C14, and C15. In addition, a control bit is provided in the memory map which enables the M13X to generate an extra clock cycle during the C3 bit time. When the $\overline{M13X}$ lead is tied low, the transmit PMDL controller can be enabled through software control. The transmit PMDL controller supports transmission of HDLC (High Level Data Link Control) encapsulated messages of arbitrary length. Interrupt request bits are provided for signaling transmit PMDL FIFO and message status. When the transmit PMDL controller is enabled, C13, C14, and C15 on the transmit C-bit interface are ignored; instead, C13, C14, and C15 are sourced from the transmit PMDL controller.

A receive C-bit interface is provided for extraction of 14 C-bits (C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, C21). The receive C-bit interface consists of a serial data output (CDR), an output clock (CCKR), a data link indicator pulse (CDCCR), and an output framing pulse (CFMR). The data link indicator pulse identifies the location of the three data link C-bits, C13, C14, and C15.

C1	C2*	C3**	C1 = C-bit parity mode
			C2 = Reserved
			C3 = Far End Alarm and Control (FEAC)
C4*	C5*	C6*	Not defined, set to 1
C7	C8	C9	C-bit Parity bits
C10	C11	C12	Far End Block Error (FEBE)
C13***	C14***	C15***	Maintenance data link (28 kbit/s)
C16*	C17*	C18*	Not defined, set to 1
C19*	C20*	C21*	Not defined, set to 1

Notes:

* These bits are always provided at the C-bit interface in the C-bit mode.

** This bit is always provided at the receive C-bit interface in the C-bit mode. This bit is optionally processed at the transmit C-bit interface.

*** These bits are always provided at the receive C-bit interface in the C-bit mode.
In the transmit direction these bits can optionally be supplied via the integrated PMDL controller.

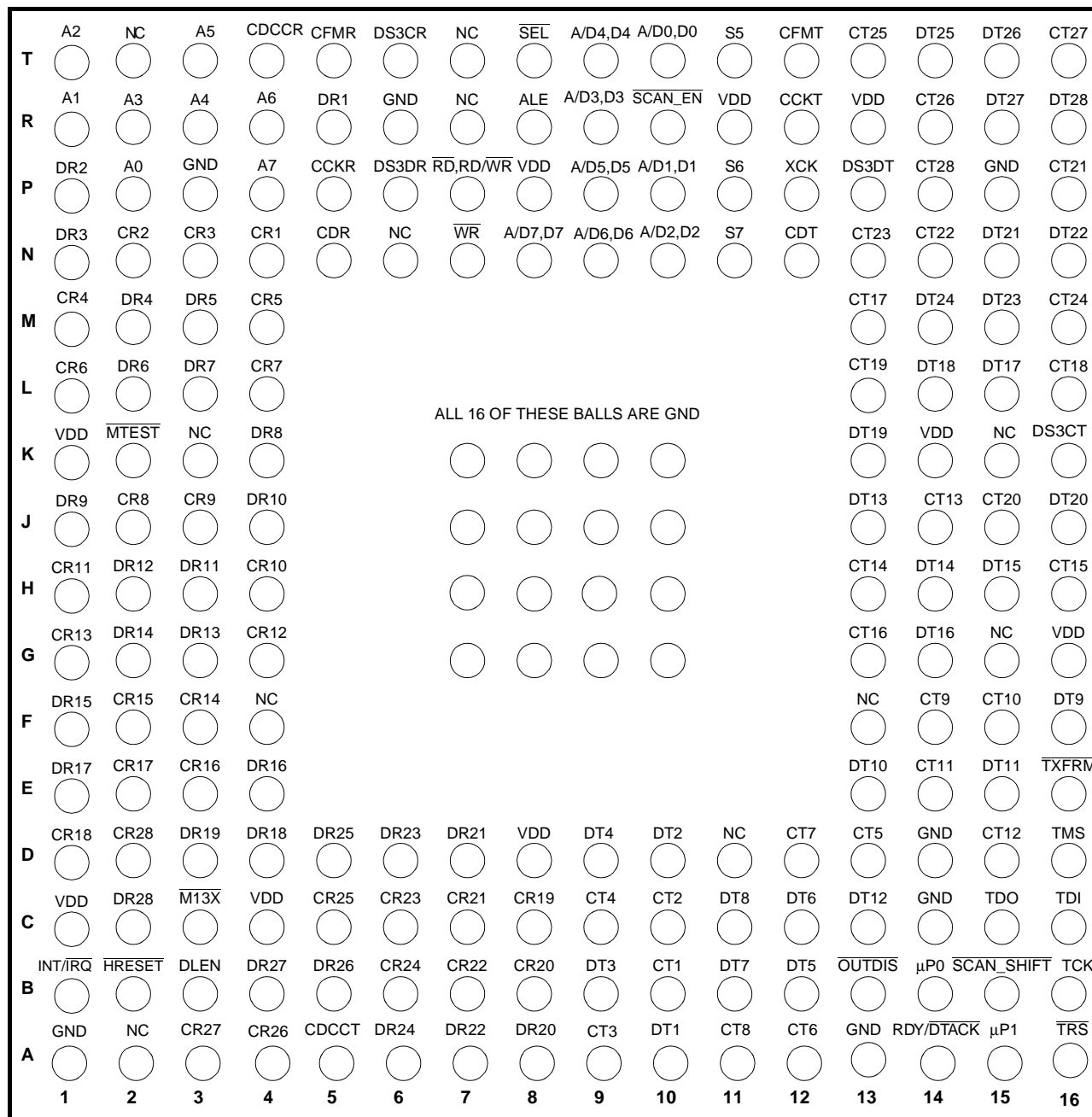**Figure 2. C-Bit Assignments**

Of the eight remaining C-bits, C1 is used as an identification channel; C3 is defined as a Far End Alarm and Control (FEAC) bit and is controlled via the memory map; C7, C8, and C9 are used for C-bit parity; and the remaining three bits, C10, C11, and C12, are used to transmit a FEBE indication. A FEBE is automatically transmitted if a C-bit parity error or framing error is received.

Fixed DS2 to DS3 stuffing is used for M23 multiplexing at a rate of seven stuffs for every 18 DS3 stuff opportunities. This yields a DS2 frequency of +2.6 ppm above the desired frequency of 6.312 Mbit/s. After adding this to the tolerance of the DS3 clock signal, ±20 ppm, the frequency is still within the ±32 ppm allowed for a DS2 signal.

Under software control, the M13X can generate DS3 idle and AIS signals, and loop back the transmitted DS3 signal to the receiver for test purposes. Other functions provided by the M13X include: DS1 loopback capability, and transmit clock failure protection. The microprocessor interface is selectable via two external hardware straps. Interface options are: Multiplexed, Intel compatible, or Motorola compatible. An interrupt request lead with programmable polarity is provided and can be used when the $\overline{\text{M13X}}$ lead is tied low.

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LEAD DIAGRAMS

The M13X is available in both plastic ball grid array (PBGA) and plastic quad flat package (PQFP) packages, as shown in Figures 3, 4, 27 and 28.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
T	A2	NC	A5	CDCCR	CFMR	DS3CR	NC	SEL	A/D4,D4	A/D0,D0	S5	CFMT	CT25	DT25	DT26	CT27
R	A1	A3	A4	A6	DR1	GND	NC	ALE	A/D3,D3	SCAN_EN	VDD	CCKT	VDD	CT26	DT27	DT28
P	DR2	A0	GND	A7	CCKR	DS3DR	RD,RD/WR	VDD	A/D5,D5	A/D1,D1	S6	XCK	DS3DT	CT28	GND	CT21
N	DR3	CR2	CR3	CR1	CDR	NC	WR	A/D7,D7	A/D6,D6	A/D2,D2	S7	CDT	CT23	CT22	DT21	DT22
M	CR4	DR4	DR5	CR5									CT17	DT24	DT23	CT24
L	CR6	DR6	DR7	CR7									CT19	DT18	DT17	CT18
K	VDD	MTEST	NC	DR8									DT19	VDD	NC	DS3CT
J	DR9	CR8	CR9	DR10									DT13	CT13	CT20	DT20
H	CR11	DR12	DR11	CR10									CT14	DT14	DT15	CT15
G	CR13	DR14	DR13	CR12									CT16	DT16	NC	VDD
F	DR15	CR15	CR14	NC									NC	CT9	CT10	DT9
E	DR17	CR17	CR16	DR16									DT10	CT11	DT11	TXFRM
D	CR18	CR28	DR19	DR18	DR25	DR23	DR21	VDD	DT4	DT2	NC	CT7	CT5	GND	CT12	TMS
C	VDD	DR28	M13X	VDD	CR25	CR23	CR21	CR19	CT4	CT2	DT8	DT6	DT12	GND	TDO	TDI
B	INT/IRQ	HRESET	DLEN	DR27	DR26	CR24	CR22	CR20	DT3	CT1	DT7	DT5	OUTDIS	µP0	SCAN_SHIFT	TCK
A	GND	NC	CR27	CR26	CDCCT	DR24	DR22	DR20	CT3	DT1	CT8	CT6	GND	RDY/DTACK	µP1	TRS

ALL 16 OF THESE BALLS ARE GND

Note: This a bottom view of the M13X 208-lead plastic ball grid array package. All leads are solder balls. Some lead symbols may be abbreviated. See Figure 27 for package dimension information. This diagram is rotated relative to the bottom view shown in Figure 27.

Figure 3. M13X TXC-03305 Lead Diagram for PBGA Package

M13X

TXC-03305AIPQ
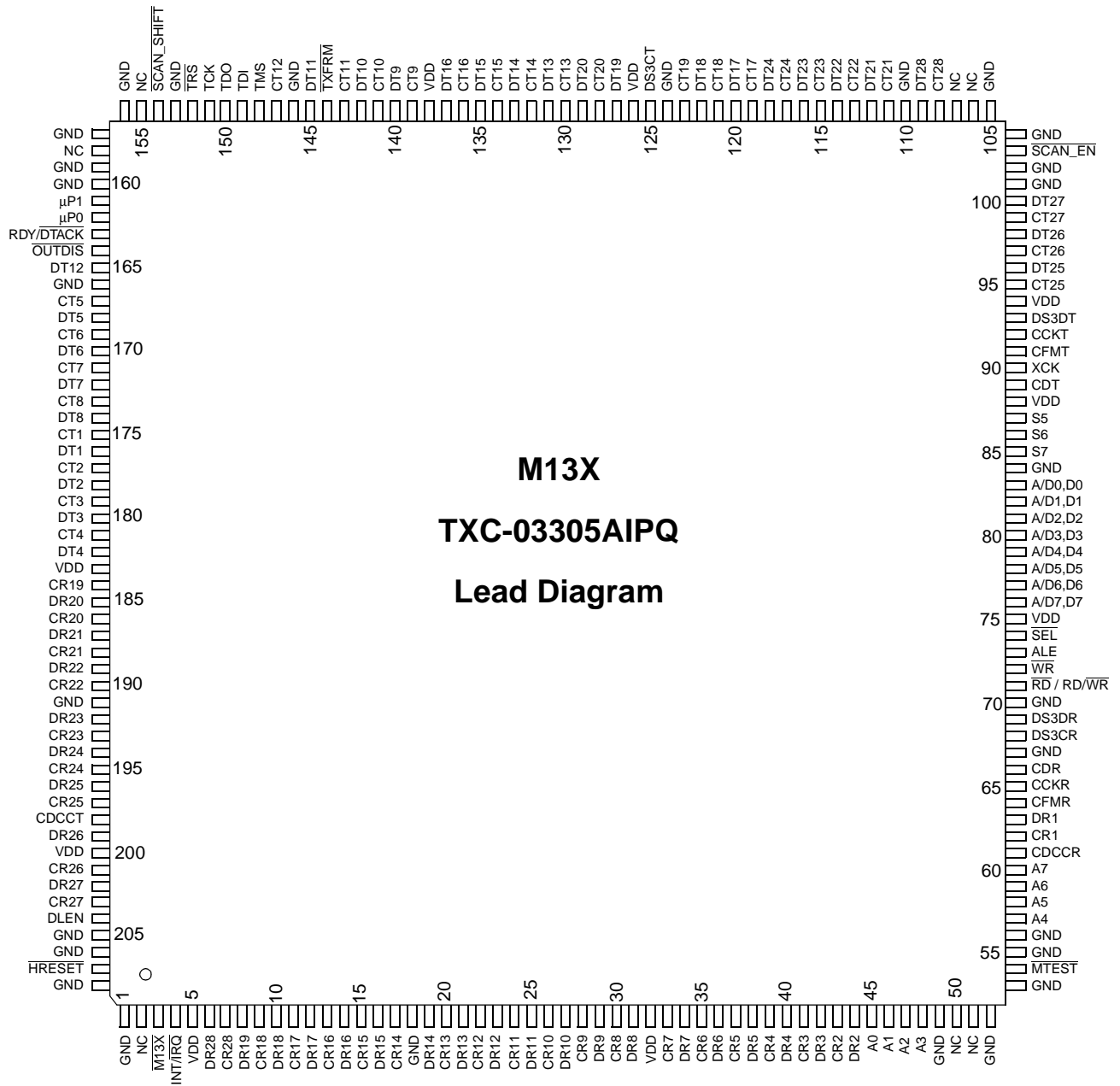
Lead Diagram

Note: This a top view of the M13X 208-lead plastic quad flat package. Some lead symbols may be abbreviated. See Figure 28 for package dimension information.

Figure 4. M13X TXC-03305 Lead Diagram for PQFP Package

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LEAD DESCRIPTIONS

All TTL8mA I/Os are slew rate controlled except for the DS3DT and DS3CT outputs.

POWER SUPPLY, GROUND, AND NO CONNECT

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P*	Type**	Name/Function
VDD	C1, C4, D8, G16, K1, K14, P8, R11, R13	5, 32, 75, 88, 94, 126, 138, 183, 200	P		**VDD:** +5-volt supply voltage, ±5%.
GND	A1, A13, C14, D14, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, P3, P15, R6	1, 18, 49, 52, 53, 55, 56, 67, 70, 84, 101, 102, 104, 105, 110, 124, 146, 153, 156, 157, 159, 160, 166, 191, 205, 206, 208	P		**Ground:** 0 volts reference.
NC	A2, D11, F4, F13, G15, K3, K15, N6, R7, T2, T7	2, 50, 51, 106, 107, 155, 158	--		**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of NC leads may impair performance or cause damage to the device. If future revisions of the device are made, then these leads may have functions associated with them.

Notes for lead descriptions tables:
* I = Input; O = Output; P = Power
** See Input, Output and Input//Output Parameters section below for Type definitions.

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DS1 RECEIVE INTERFACES

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
CR1	N4	62	O	TTL2mA	**Receive DS1 Clocks, Channels 1 - 28:** Receive
CR2	N2	43			data is clocked out of the M13X on rising edges of
CR3	N3	41			these clocks. The clock for the first DS1 channel
CR4	M1	39			corresponds to CR1, while the clock for the last
CR5	M4	37			DS1 channel corresponds to CR28. During normal
CR6	L1	35			operation, the DS1 clock signals are derived from
CR7	L4	33			the DS3 clock signal (DS3CR) and are stretched
CR8	J2	30			due to overhead and stuff bit removal. When the
CR9	J3	28			$\overline{\text{M13X}}$ lead is tied low and the DJB control bit is set
CR10	H4	26			to a 1, the internal DJB circuits will be enabled,
CR11	H1	24			which will reduce the amount that these clocks are
CR12	G4	22			stretched, thereby reducing their jitter. During cer-
CR13	G1	20			tain DS3 alarm conditions (programmable via
CR14	F3	17			1TAIS1 and 1TAIS0, bits 5 and 4 in register 20H)
CR15	F2	15			the M13X provides a DS1 clock signal for clocking
CR16	E3	13			out AIS which is derived from the XCK clock lead.
CR17	E2	11			
CR18	D1	9			
CR19	C8	184			
CR20	B8	186			
CR21	C7	188			
CR22	B7	190			
CR23	C6	193			
CR24	B6	195			
CR25	C5	197			
CR26	A4	201			
CR27	A3	203			
CR28	D2	7			

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
DR1	R5	63	O	TTL2mA	**Receive DS1 Data, Channels 1 - 28:** Demulti-
DR2	P1	44			plexed DS1 channels. The first DS1 channel corre-
DR3	N1	42			sponds to DR1, while the last DS1 channel
DR4	M2	40			corresponds to DR28. During normal operation
DR5	M3	38			these data outputs are stretched due to overhead
DR6	L2	36			and stuff bit removal. When the $\overline{M13X}$ lead is tied
DR7	L3	34			low and the DJB bit is set to a 1, the internal DJB
DR8	K4	31			circuits will be enabled, which will reduce the
DR9	J1	29			amount that these data outputs are stretched,
DR10	J4	27			thereby reducing their jitter.
DR11	H3	25			
DR12	H2	23			
DR13	G3	21			
DR14	G2	19			
DR15	F1	16			
DR16	E4	14			
DR17	E1	12			
DR18	D4	10			
DR19	D3	8			
DR20	A8	185			
DR21	D7	187			
DR22	A7	189			
DR23	D6	192			
DR24	A6	194			
DR25	D5	196			
DR26	B5	199			
DR27	B4	202			
DR28	C2	6			

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DS1 TRANSMIT INTERFACES

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
CT1	B10	175	I	TTL	**Transmit DS1 Clocks, Channels 1 - 28:** Transmit data is clocked into the M13X on either the rising or falling edges of these clocks, depending on the setting of the INVCK bit. The clock for the first DS1 channel corresponds to CT1, while the clock for the last DS1 channel corresponds to CT28.
CT2	C10	177			
CT3	A9	179			
CT4	C9	181			
CT5	D13	167			
CT6	A12	169			
CT7	D12	171			
CT8	A11	173			
CT9	F14	139			
CT10	F15	141			
CT11	E14	143			
CT12	D15	147			
CT13	J14	130			
CT14	H13	132			
CT15	H16	134			
CT16	G13	136			
CT17	M13	119			
CT18	L16	121			
CT19	L13	123			
CT20	J15	128			
CT21	P16	111			
CT22	N14	113			
CT23	N13	115			
CT24	M16	117			
CT25	T13	95			
CT26	R14	97			
CT27	T16	99			
CT28	P14	108			

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Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
DT1	A10	176	I	TTL	**Transmit DS1 Data, Channels 1 - 28:** The first
DT2	D10	178			DS1 channel corresponds to DT1, while the last
DT3	B9	180			DS1 channel corresponds to DT28.
DT4	D9	182			
DT5	B12	168			
DT6	C12	170			
DT7	B11	172			
DT8	C11	174			
DT9	F16	140			
DT10	E13	142			
DT11	E15	145			
DT12	C13	165			
DT13	J13	131			
DT14	H14	133			
DT15	H15	135			
DT16	G14	137			
DT17	L15	120			
DT18	L14	122			
DT19	K13	127			
DT20	J16	129			
DT21	N15	112			
DT22	N16	114			
DT23	M15	116			
DT24	M14	118			
DT25	T14	96			
DT26	T15	98			
DT27	R15	100			
DT28	R16	109			

DS3 INTERFACE

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
DS3CR	T6	68	I	CMOS	**DS3 Receive Clock:** A 44.736 MHz clock that is used to clock DS3 data into the M13X. This clock is used as the time base for demultiplexing the DS3 data. When the loop timing feature is active (a 1 written into bit 3 (LPTIME) in 02H), or when the DS3 external transmit clock (XCK) fails, this clock becomes the transmit clock.
DS3DR	P6	69	I	CMOS	**DS3 Receive Data:** Receive 44.736 Mbit/s data is clocked into the M13X on rising edges of the receive clock (DS3CR).
DS3CT	K16	125	O	TTL8mA[1]	**DS3 Transmit Clock:** A 44.736 MHz clock which is derived from the external transmit clock input signal (XCK) or from the DS3 Receive Clock (DS3CR) when loop timing mode is enabled or when the XCK clock fails. It is used to clock DS3 data from the M13X.
DS3DT	P13	93	O	TTL8mA[2]	**DS3 Transmit Data:** Transmit C-bit parity or M13 formatted DS3 data is clocked out of the M13X on rising edges of the transmit clock (DS3CT).
$\overline{\text{TXFRM}}$	E16	144	I	TTLp	**Transmit DS3 Frame Synchronization Pulse:** An active low pulse that is sampled on the rising edge of the transmit DS3 clock (XCK or DS3CR), and is used to align the transmit DS3 frame. The X1 bit of the transmit DS3 frame is three clocks delayed with respect to the $\overline{\text{TXFRM}}$. The use of this lead is optional. If it is not used then it must either be left floating or pulled high.

Notes:

1. DS3CT is not slew rate limited.

2. DS3DT is not slew rate limited.

MICROPROCESSOR INTERFACE

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
μP1 μP0	A15 B14	161 162	I	TTLp	**Microprocessor Interface Type Select:** The type of microprocessor interface selected by these two bits is given in the table below: | μP1	μP0	Interface
---	---	---
High	High	Multiplexed (only allowed when $\overline{M13X}$ lead is high)
High	Low	Multiplexed
Low	Low	Intel Compatible
Low	High	Motorola Compatible	 The multiplexed interface consists of eight bidirectional address/data leads, select, address latch enable, read, write and interrupt request. When μP(1-0) = H,H only address range 00H-1FH is accessible, address straps S5-S7 are active, and the $\overline{M13X}$ lead must be left floating or tied high. This enables backwards compatibility of the 208-lead PQFP packaged devices with the predecessor M13E device that has the same package and lead assignments. It also enables functional compatibility with the earlier M13 device, which has a 160-lead PQFP package. When μP(1-0) = H,L only address range 00H-3FH is accessible, address straps S6-S7 are active and the state of the $\overline{M13X}$ lead determines whether the M13X functionality in registers 25H-3FH is enabled or disabled. The Intel compatible interface (80X86 family) consists of eight address leads, eight bidirectional data leads, select, read, write, ready and interrupt request. The Motorola compatible interface (680X0 family) consists of eight address leads, eight bidirectional data leads, select, read/write, data transfer acknowledge and interrupt request. For both the Intel and Motorola compatible interfaces, registers 00H-24H are accessible if $\overline{M13X}$ is high and registers 00H-3FH are accessible if $\overline{M13X}$ is low. Address straps S6-S7 are active.

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
S7 S6 S5	N11, P11, T11	85, 86, 87	I	TTLp	**Address Straps:** When the Intel, Motorola, or Multiplexed (μP1 is high and μP0 is low) microprocessor interfaces are selected, the two address straps, S7 and S6, allow the M13X to be partitioned as a segment of memory. The straps define the address offset of the device. The address register is partitioned as shown below. The data register pointed to by the 6 least significant bits is only accessed if the 2 most significant bits match the address straps. Address register partition for Intel, Motorola, or Multiplexed (μP1 is high and μP0 is low) microprocessor interfaces: Bit 7 6 M13X Address / Register Address When the multiplexed microprocessor interface is selected, by setting μP1 high and μP0 high, the three address straps, S7, S6, and S5, allow the M13X to be partitioned as a segment of memory. The straps define the offset of the device. The address register is partitioned as shown below. The data register pointed to by the five least significant bits is only accessed if the three most significant bits match the address straps. Address register partition for the multiplexed microprocessor interface when μP1 is high and μP0 is high: Bit 7 6 5 M13X Address / Register Address
A7 A6 A5 A4 A3 A2 A1 A0	P4 R4 T3 R3 R2 T1 R1 P2	60 59 58 57 48 47 46 45	I	TTLp	**Address Bus (Intel/Motorola):** Multiplexed - These leads are disabled when the multiplexed interface is selected. Intel/Motorola - These are active high address line inputs that are used by the microprocessor for accessing the M13X registers for a read/write cycle. A7 is the most significant bit.
A/D7 D7 A/D6 D6 A/D5 D5 A/D4 D4 A/D3 D3 A/D2 D2 A/D1 D1 A/D0 D0	N8 N9 P9 T9 R9 N10 P10 T10	76 77 78 79 80 81 82 83	I/O	TTL8mA	**Address/Data Bus (Multiplexed) or Data Bus (Intel/Motorola):** Multiplexed - These bidirectional leads constitute address/data buses for accessing the M13X registers. Intel/Motorola - These bidirectional leads are used only for transferring data. The most significant bit is A/D7 or D7.

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Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
$\overline{SEL}$	T8	74	I	TTL	**Select:** A low enables data transfers between the microprocessor and the M13X registers during a read/write bus cycle.
$\overline{RD}$ RD/$\overline{WR}$	P7	71	I	TTL	**Read (Intel/Multiplexed) or Read/Write (Motorola):** Intel/Multiplexed - An active low signal generated by the microprocessor for reading the M13X register locations. Motorola - An active high signal generated by the microprocessor for reading the M13X register locations. An active low signal is used to write to the M13X register locations.
ALE	R8	73	I	TTL	**Address Latch Enable (Multiplexed):** Multiplexed - An active high enable signal generated by the microprocessor. The falling edge is used to store an address during a read/write bus cycle. Intel/Motorola - not used. This lead should be tied low when not used.
$\overline{WR}$	N7	72	I	TTL	**Write (Intel/Multiplexed):** Intel/Multiplexed - An active low signal generated by the microprocessor for writing to the M13X register locations. Motorola - not used. This lead should be tied high when not used.
RDY/ $\overline{DTACK}$	A14	163	O	TTL8mA	**Ready (Intel) or Data Transfer Acknowledge (Motorola):** Intel/Multiplexed - This output lead is not used, and it is always high when the $\overline{SEL}$ lead is low, otherwise it is tri-stated. Connection to an Intel microprocessor is optional. If connected, a pull-up resistor is required. Motorola - During a read bus cycle, a low signal indicates the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data. A pull-up resistor is required for this lead.
INT/$\overline{IRQ}$	B1	4	O	TTL8mA	**Interrupt Request:** This is a tri-state interrupt request lead. This lead is tri-stated when not being driven active. When this lead is driven active, the IPOLAL bit (bit 6 in register 3DH) determines the polarity of this lead. This lead will be driven active when an interrupt request bit AND its corresponding interrupt request mask bit are both set to a 1. An external pull-up or pull-down resistor is required to pull this lead to the proper inactive level when it is not being driven.

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RECEIVE C-BIT INTERFACE

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
CCKR	P5	65	O	TTL8mA	**Receive C-Bit Clock:** A gapped clock signal is provided for clocking out the selected receive C-bit data. Data (CDR) is clocked out on the rising edges of CCKR.
CDR	N5	66	O	TTL8mA	**Receive C-Bit Data:** The following C-bits are provided at this interface: C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21.
CFMR	T5	64	O	TTL8mA	**Receive C-Bit Framing Pulse:** This positive framing pulse occurs prior to the C2 bit.
CDCCR	T4	61	O	TTL8mA	**Receive Data Link Indication:** A positive pulse that identifies the location of the three data link C-bits (C13, C14, and C15). The receive C-bit clock (CCKR) may be and-gated with this signal to provide a gapped data link clock signal for loading the three C-bits from the C-bit data (CDR) into external circuitry, such as in M13E device applications. This signal is not needed if the internal HDLC controller is used since the C13, C14, and C15 C-bits are then processed internally. This signal is enabled by placing a high on the DLEN input signal lead.

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TRANSMIT C-BIT INTERFACE

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
CCKT	R12	92	O	TTL8mA	**Transmit C-Bit Clock:** A gapped clock signal is provided for clocking in selected transmit C-bit data (CDT). Data is clocked into the M13X on the rising edges of CCKT.
CDT	N12	89	I	TTL	**Transmit C-Bit Data:** The transmit gapped clock (CCKT) is provided for clocking in the following C-bits: C2, C3 (depending on the setting of bit 7 of register 19H, C3CLKI), C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. An unused C-bit should be transmitted as a 1. C13, C14, and C15 are sourced by the transmit PMDL controller when it is enabled, even though the clock pulses for C13, C14, and C15 are still present.
CFMT	T12	91	O	TTL8mA	**Transmit C-Bit Framing Pulse:** This positive framing pulse occurs prior to the C2 bit.
CDCCT	A5	198	O	TTL8mA	**Transmit Data Link Indication:** A positive pulse that identifies the location of the three data link C-bits (C13, C14, and C15). The transmit C-bit clock (CCKT) may be and-gated with this signal to provide a gapped data link clock signal for PMDL applications where it is desired to use an external HDLC controller instead of the on-chip HDLC controller, such as in existing M13E device applications. This signal is not needed if the internal HDLC controller is used. This signal is enabled by placing a high on the DLEN input signal lead.

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CONTROL LEADS

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
OUTDIS	B13	164	I	TTLp	**Outputs Disable:** A low causes all M13X outputs and bidirectional signal leads to be set to a high impedance state for test purposes except the TDO, CDCCR and CDCCT leads. The CDCCR and CDCCT leads can be tri-stated by applying a low to the DLEN lead. This lead is provided with an internal pull-up resistor.
DLEN	B3	204	I	TTLp	**Data Link Enable:** Normally left open. A high enables the transmit and receive data link indication signals, CDCCT and CDCCR. The data link indication signals identify the location of the three data link C-bits (C13, C14, and C15). This lead is provided with an internal pull-up resistor.
HRESET	B2	207	I	TTLp	**Asynchronous Device RESET:** This active low lead should be toggled low for a minimum of 25 ns and then high after the power to the M13X has stabilized, to perform a global reset of the M13X device. When a global reset occurs, the memory map is initialized to all 0s except for the XT and T2X1-T2X7 bits which are set to 1s, and internal circuitry is reset. This lead is provided with an internal pull-up resistor.
M13X	C3	3	I	TTLp	**Enable M13X Functions:** When this input lead is high, the M13X device has the same functionality as the M13E device. Also, the TXFRM lead and ID bit can be used as well. All M13X functions in registers 25H-3FH are disabled and all counters are 8 bits long. When this lead is low, the M13X functions in registers 25H-3FH are enabled (i.e., all features of the device can be used), and all counters become 16 bits long. This lead is provided with an internal pull-up resistor. When the M13X lead is low, the NEW bit in register 1DH does not become set to one again after it is cleared when a continuous constant FEAC message is received.

EXTERNAL CLOCK

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
XCK	P12	90	I	CMOS	**External Transmit Clock:** An external clock having a frequency of 44.736 MHz and a stability of ±20 ppm is required to meet DSX-3 cross-connect requirements. The clock duty cycle should be kept to $(50\pm5)\%$. The transmit clock is also used to operate the M13X microprocessor interface. The M13X monitors this clock for transitions. When a clock failure is detected, the M13X automatically switches to the receive clock (DS3CR) for multiplexer and microprocessor operation. Receive loop timing (a 1 written to bit 3, LPTIME, in 02H) also causes the receive clock to become the transmit clock.

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TEST ACCESS PORT

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
TMS	D16	148	I	TTLp	**Test Mode Select:** The signal present on this lead is used to control boundary scan test operations. This lead is provided with an internal pull-up resistor.
TDI	C16	149	I	TTLp	**Test Data Input:** Serial data input for boundary scan test messages. This lead is provided with an internal pull-up resistor.
TDO	C15	150	O	TTL8mA	**Test Data Output:** Serial data output whose information is clocked out on falling edges of TCK.
TCK	B16	151	I	TTLp	**Test Clock:** The input clock for boundary scan testing. The TDI and TMS states are clocked in on its rising edges. This lead is provided with an internal pull-up resistor.
$\overline{\text{TRS}}$	A16	152	I	TTLp	**Test Reset:** When an active low signal is applied to this lead, the M13X Test Access Port (TAP) controller resets and the boundary scan is disabled. The controller is also reset by holding the TMS signal lead high for at least five rising clock edges of TCK. During power-up of the M13X, this lead must be held low, to reset the TAP controller. Failure to do so may cause the TAP controller to take control of the M13X output leads. When the boundary scan feature is not used, this lead must be tied low. The software reset function in register 1FH does not affect the boundary scan logic. This lead is provided with an internal pull-up resistor.

SCAN TEST LEADS

Symbol	Lead No. BGA	Lead No. PQFP	I/O/P	Type	Name/Function
$\overline{\text{MTEST}}$	K2	54	I	TTLp	**Scan Test:** Leave disconnected.
$\overline{\text{SCAN\_EN}}$	R10	103	I	TTLp	**Scan Test:** Leave disconnected.
$\overline{\text{SCAN\_SHIFT}}$	B15	154	I	TTLp	**Scan Test:** Leave disconnected.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+6.0	V	Note 1
DC input voltage	V_{IN}	-0.3	V_{DD} + 0.3	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	Absolute value 2000		V	Note 3
LATCH-UP	LU				Meets JEDEC JC-40.2

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, method 3015.7.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient of PBGA Package.			38	$^oC/W$	0 ft/min linear airflow
Thermal resistance - junction to ambient of PQFP Package.			26	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			150.5	mA	
P_{DD}			790	mW	Inputs switching and worst case process and loading.

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INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

All rise times are measured from 0 to 1.4V and all fall times are measured from V_{DD} to 1.4V.

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.7 x V_{DD}			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.3 x V_{DD}	V	4.75 ≤ V_{DD} ≤ 5.25
Input leakage current			±10	µA	V_{DD} = 5.25; Input = 0 to 5.25V
Input capacitance		4		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤ V_{DD} ≤ 5.25
Input leakage current			±10	µA	V_{DD} = 5.25; Input = 0 to 5.25V
Input capacitance		4		pF	

INPUT PARAMETERS FOR TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤ V_{DD} ≤ 5.25
Input leakage current		-0.1	-0.35	mA	V_{DD} = 5.25; Input = 0 V
Input capacitance		4		pF	

Note: The TTLp input has a 50kΩ (nominal) internal pull-up resistor.

OUTPUT PARAMETERS FOR TTL2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-1.0	mA	
t_{RISE}		4.6		ns	C_{LOAD} = 15 pF
t_{FALL}		4.3		ns	C_{LOAD} = 15 pF
Tri-state leakage current			±10	µA	V_{DD} = 5.25

INPUT/OUTPUT PARAMETERS FOR TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 $\leq V_{DD} \leq$ 5.25
V_{IL}			0.8	V	4.75 $\leq V_{DD} \leq$ 5.25
Input leakage current			±10	µA	V_{DD} = 5.25; Input = 0 to 5.25V
Input capacitance		5.5		pF	
V_{OH}	2.4			V	V_{DD} = 4.75; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE} (Note 1)		2.4		ns	C_{LOAD} = 25 pF
t_{FALL} (Note 1)		2.4		ns	C_{LOAD} = 25 pF
t_{RISE} (Note 2)		2.7		ns	C_{LOAD} = 25 pF
t_{FALL} (Note 2)		2.7		ns	C_{LOAD} = 25 pF
Tri-state leakage current			±10	µA	V_{DD} = 5.25

Notes:

1. This parameter only applies to DS3CT and DS3DT.
2. This parameter applies to all TTL8mA I/Os except for DS3CT and DS3DT.

TIMING CHARACTERISTICS

Detailed timing diagrams for the M13X are illustrated in the Figures 5 through 18 below with values of the timing intervals tabulated below each waveform diagram. All output times are measured with a maximum of 15 pF load capacitance for TTL 2 mA outputs and 25 pF load capacitance for TTL 8 mA outputs. Timing parameters are measured at voltage levels of $V_{DD}/2$ for CMOS input signals or 1.4 V for all TTL input and output signals.

Figure 5. DS3 Receive Timing
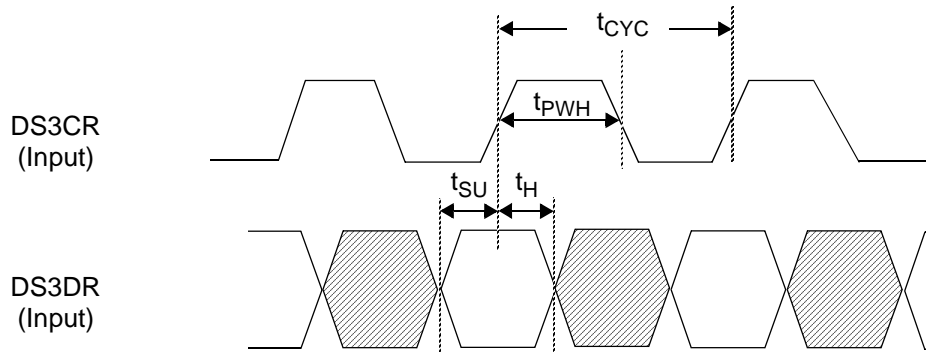
Parameter	Symbol	Min	Typ	Max	Unit
DS3CR clock period	t_{CYC}	20.0	22.35		ns
DS3CR duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
DS3DR setup time before DS3CR↑	t_{SU}	-1.0			ns
DS3DR hold time after DS3CR↑	t_H	6.0			ns

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Figure 6. DS3 Transmit Timing
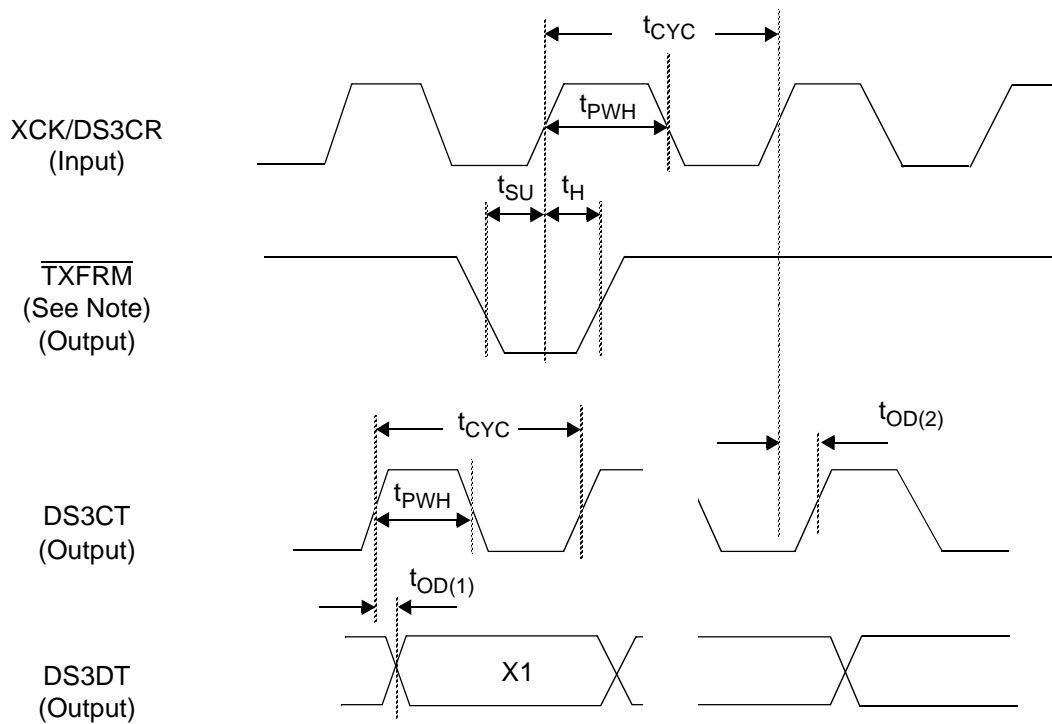
Note: $\overline{\text{TXFRM}}$ is sampled by XCK or DS3CR, whichever is the current transmit clock.
The X1 bit of DS3DT is three (3) clock cycles (of XCK/DS3CR) delayed with respect to $\overline{\text{TXFRM}}$.

Parameter	Symbol	Min	Typ	Max	Unit
XCK/DS3CR or DS3CT clock period	t_{CYC}	20	22.35		ns
XCK/DS3CR or DS3CT duty cycle (t_{PWH}/t_{CYC})	--	45	50	55	%
DS3DT output delay after DS3CT↑	$t_{OD(1)}$	2.0		8.0	ns
DS3CT↑ output delay after XCK/DS3CR↑	$t_{OD(2)}$	5.0		17	ns
$\overline{\text{TXFRM}}$ setup time before XCK/DS3CR↑	t_{SU}	1.0			ns
$\overline{\text{TXFRM}}$ hold time after XCK/DS3CR↑	t_{H}	1.2			ns

Figure 7. DS1 Receive Timing with DJBs Disabled
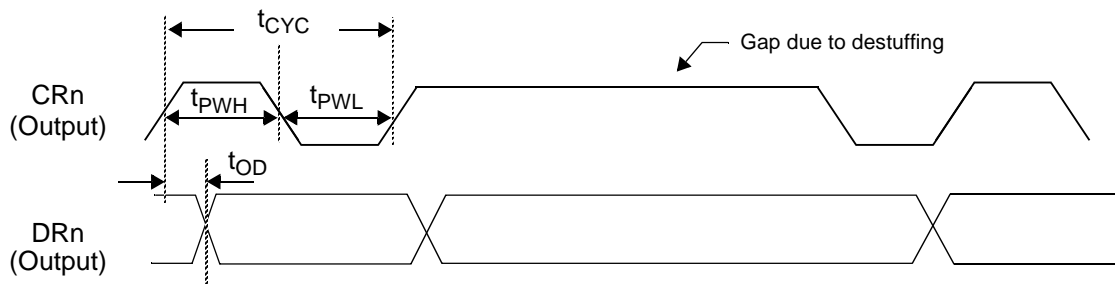
Parameter	Symbol	Min	Typ	Max	Unit
CRn clock period	t_{CYC}	28 DS3CR Cycles		64 DS3CR Cycles	ns
CRn high time	t_{PWH}	14 DS3CR Cycles		50 DS3CR Cycles	ns
CRn low time	t_{PWL}	14 DS3CR Cycles		22 DS3CR Cycles	ns
DRn output delay after CR↑	t_{OD}	-12		10	ns

Figure 8. DS1 Receive Timing with DJBs Enabled
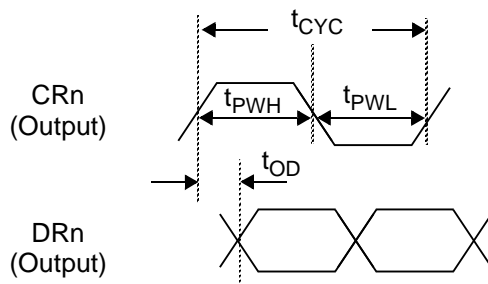
Parameter	Symbol	Min	Typ	Max	Unit
CRn clock period	t_{CYC}	28 DS3CR/XCK Cycles		29 DS3CR/XCK Cycles	ns
CRn high time	t_{PWH}	14 DS3CR/XCK Cycles		15 DS3CR/XCK Cycles	ns
CRn low time	t_{PWL}	14 DS3CR/XCK Cycles		14 DS3CR/XCK Cycles	ns
DRn output delay after CR↑	t_{OD}	-12		10	ns

Note: When the DJBS are enabled, the DS1 receive timing is derived from the transmit clock source, which can be DS3CR or XCK.

Figure 9. DS1 Transmit Timing
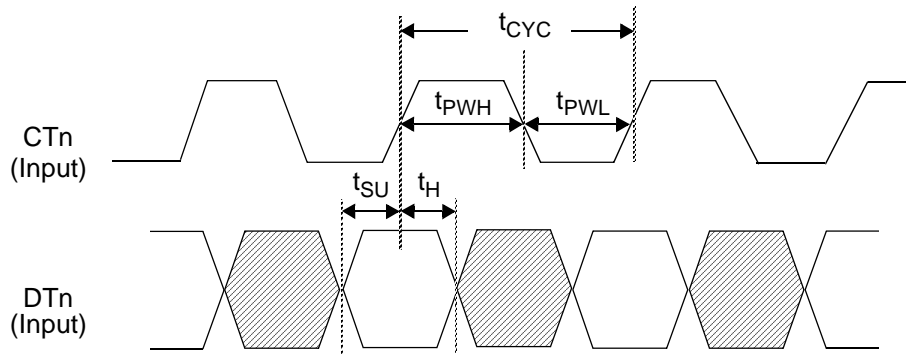
Parameter	Symbol	Min	Typ	Max	Unit
CTn clock period	t_{CYC}	583	648	1305	ns
CTn high time	t_{PWH}	145	324	--	ns
CTn low time	t_{PWL}	145	324	--	ns
DTn setup time before CT↑	t_{SU}	4.0			ns
DTn hold time after CT↑	t_H	6.0			ns

Notes:

1. Each DS1 input can be asynchronous with respect to another DS1 channel.

2. The diagram above is shown for INVCK = 0. When INVCK = 1, the DTn signals are clocked into the M13X on the falling edges of their corresponding CTn signals.

3. The timing parameters in the table above do not change when INVCK = 1 except that t_{SU} and t_H are measured with respect to the falling edges of the CTn signals.

4. The transmit DS1 inputs can accept jitter which exceeds the DS1 input jitter tolerance curve of GR-499-CORE for Category I Interface.

5. CTn clock period Max indicates the ability of the device to accept a gapped clock but does not indicate a continuous period.

Figure 10. C-Bit Receive Interface Timing
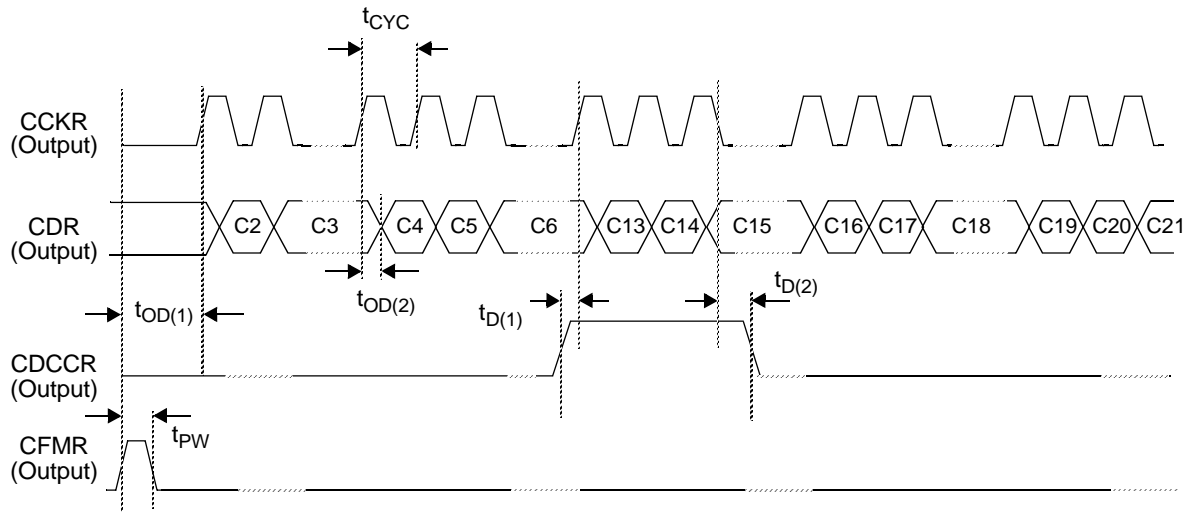
Parameter	Symbol	Min	Typ	Max	Unit
CCKR clock period	t_{CYC}		3800		ns
CCKR output delay after CFMR↑	$t_{OD(1)}$		3800		ns
CDR output delay after CCKR↑	$t_{OD(2)}$	0.5	1.0	1.5	DS3CR/ XCK clock cycle
CCKR↑ delay after CDCCR↑	$t_{D(1)}$		1900		ns
CDCCR↓ delay after CCKR↓	$t_{D(2)}$		3800		ns
CFMR pulse width (high)	t_{PW}		1900		ns

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Figure 11. C-Bit Transmit Interface Timing
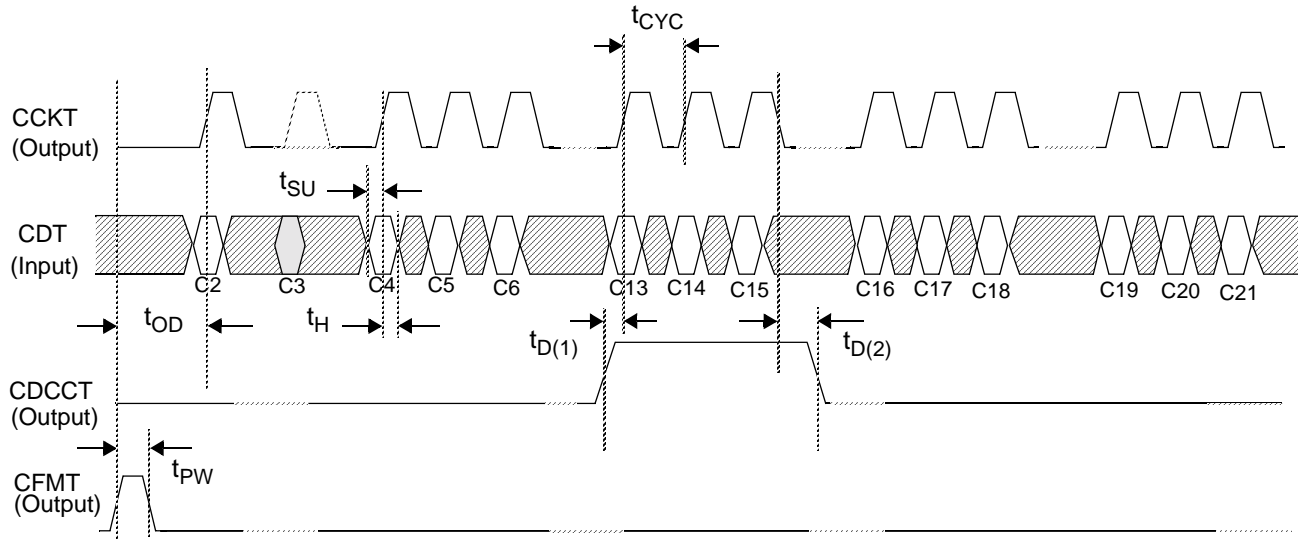
Notes:

1. A C-bit must be transmitted as a 1 when not needed.

2. Following normal power-up procedures, bit 7 in register 19H will be set to "0" and the extra clock pulse for the C3 bit in the CCKT clock will be present. If bit 7 is then set to "1," the extra C3 bit clock pulse will not be present.

Parameter	Symbol	Min	Typ	Max	Unit
CCKT clock period	t_{CYC}		3800		ns
CDT setup time before CCKT↑	t_{SU}	25			ns
CDT hold time after CCKT↑	t_H	40			ns
CCKT output delay after CFMT↑	t_{OD}		3800		ns
CCKT↑ delay after CDCCT↑	$t_{D(1)}$		1900		ns
CDCCT↓ delay after CCKT↓	$t_{D(2)}$		3800		ns
CFMT pulse width	t_{PW}		1900		ns

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Figure 12. Microprocessor Read Cycle Timing - Multiplexed Interface
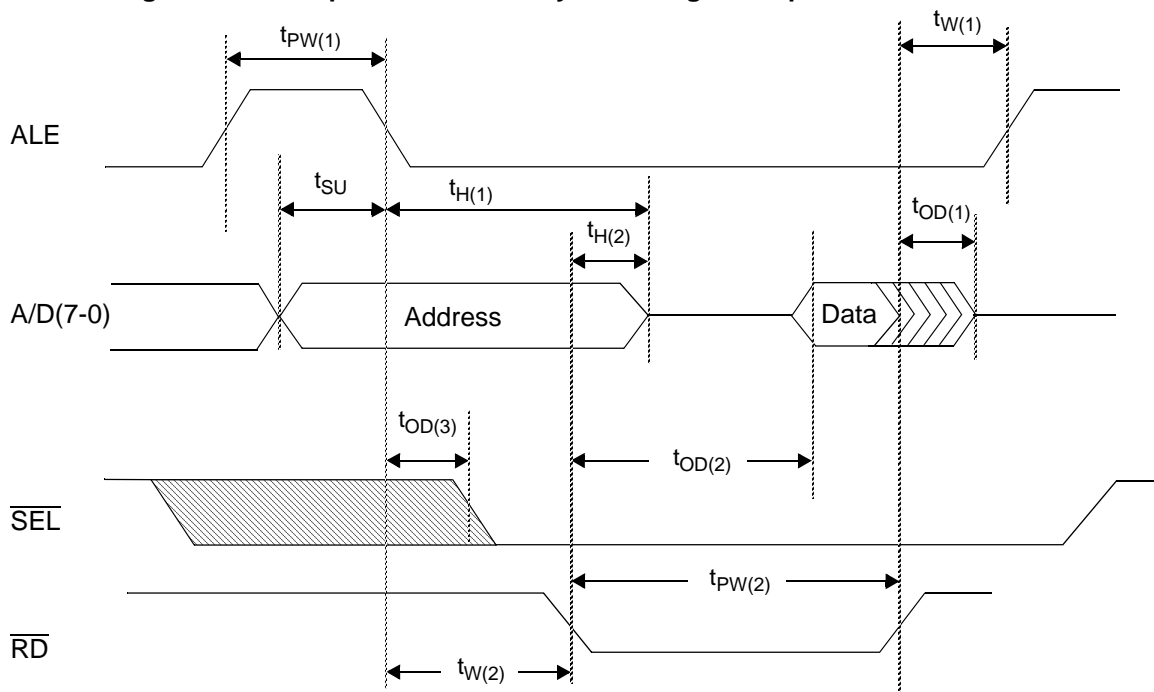
Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	95			ns
ALE wait after $\overline{RD} \uparrow$	$t_{W(1)}$	20			ns
A/D(7-0) address setup time before ALE $\downarrow$	t_{SU}	30			ns
A/D(7-0) address hold time after ALE $\downarrow$	$t_{H(1)}$	25			ns
A/D(7-0) address hold time after $\overline{RD} \downarrow$	$t_{H(2)}$			20	ns
A/D(7-0) data output delay (to tri-state) after $\overline{RD} \uparrow$	$t_{OD(1)}$	10		50	ns
A/D(7-0) data valid delay after $\overline{RD} \downarrow$	$t_{OD(2)}$			150	ns
$\overline{SEL} \downarrow$ wait after ALE $\downarrow$	$t_{OD(3)}$			80	ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	180		212,000	ns
$\overline{RD}$ wait after ALE $\downarrow$	$t_{W(2)}$	25			ns

Notes:

1. The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate. The RDY/DTACK output lead is always driven high when the $\overline{SEL}$ lead is low, otherwise it is tri-stated, which corresponds to the behavior of the M13E device.

2. The $\overline{SEL}$ lead must be brought high for 2 transmit clock cycles before the start of a new read cycle.

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Figure 13. Microprocessor Write Cycle Timing - Multiplexed Interface
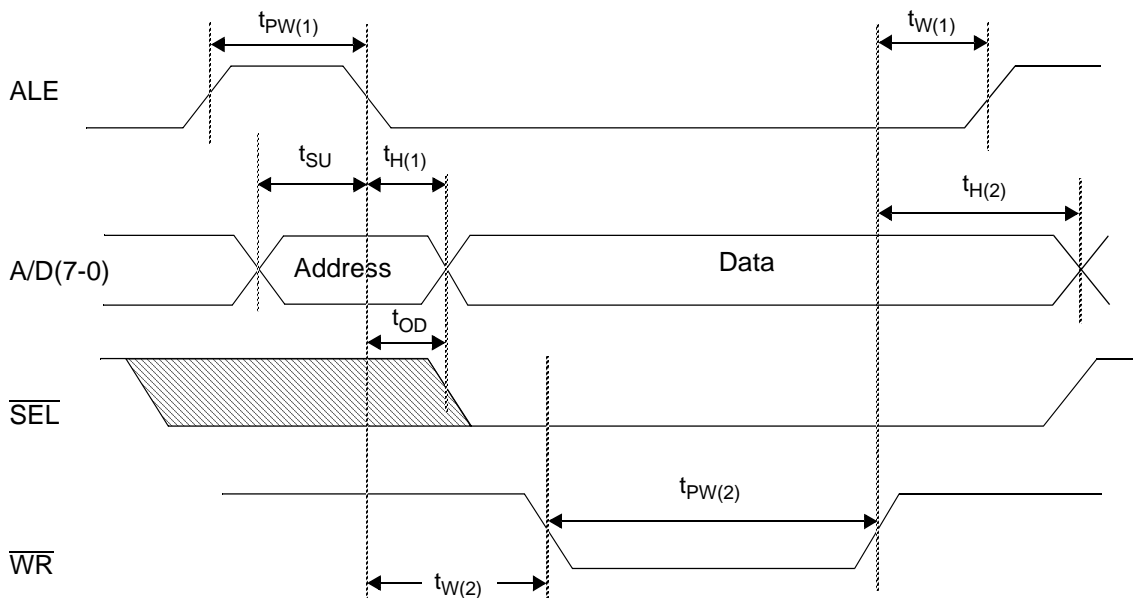
Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	95			ns
ALE wait after $\overline{WR}$ ↑	$t_{W(1)}$	20			ns
A/D(7-0) address setup time before ALE ↓	t_{SU}	30			ns
A/D(7-0) address hold time after ALE ↓	$t_{H(1)}$	25			ns
A/D(7-0) data hold time after $\overline{WR}$ ↑	$t_{H(2)}$	20			ns
$\overline{SEL}$ wait after ALE↓	t_{OD}			80	ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	200		212,000	ns
$\overline{WR}$ wait after ALE ↓	$t_{W(2)}$	25			ns

Notes:

1. The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate. The RDY/DTACK output lead is always driven high when the $\overline{SEL}$ lead is low, otherwise it is tri-stated, which corresponds to the behavior of the M13E device.

2. The $\overline{SEL}$ lead must be brought high for 2 transmit clock cycles before the start of a new write cycle.

Figure 14. Microprocessor Read Cycle Timing - Intel Interface
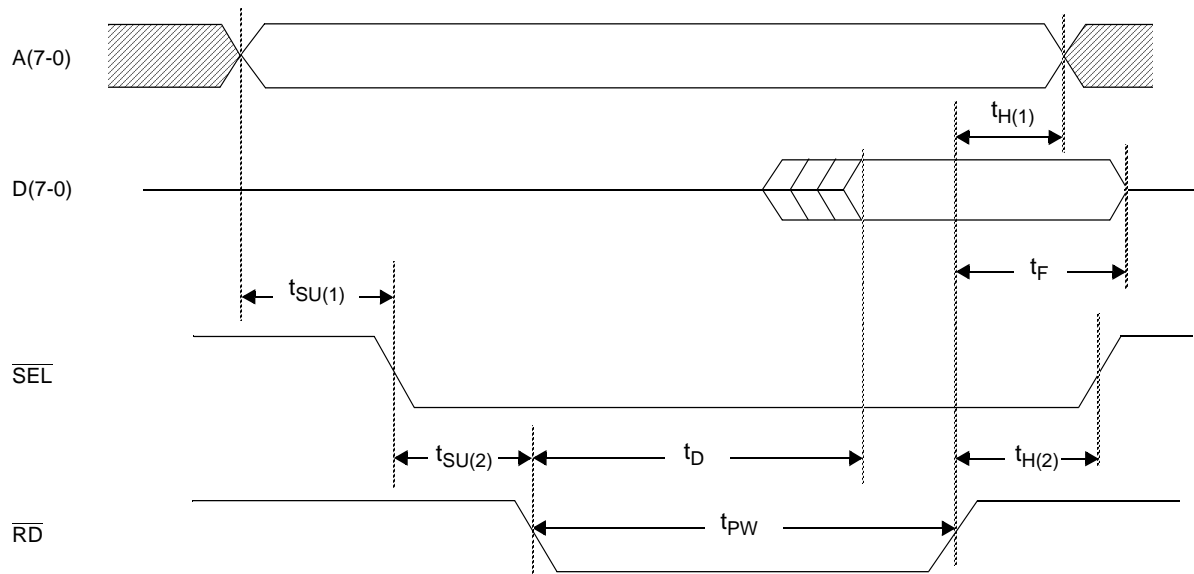
Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	0.0			ns
A(7-0) address setup time before $\overline{SEL}\downarrow$	$t_{SU(1)}$	20			ns
D(7-0) data valid delay after $\overline{RD}\downarrow$	t_D			60	ns
D(7-0) data float time after $\overline{RD}\uparrow$	t_F			80	ns
$\overline{RD}$ pulse width	t_{PW}	80		212,000	ns
$\overline{SEL}\downarrow$ setup time before $\overline{RD}\downarrow$	$t_{SU(2)}$	10			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	0.0			ns

Notes:

1. The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus
   interface to operate. The RDY/$\overline{DTACK}$ output lead is always driven high when the $\overline{SEL}$ lead is low,
   otherwise it is tri-stated, which corresponds to the behavior of the M13E device.

2. The $\overline{SEL}$ lead must be brought high for 2 transmit clock cycles before the start of a new read cycle.

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Figure 15. Microprocessor Write Cycle Timing - Intel Interface
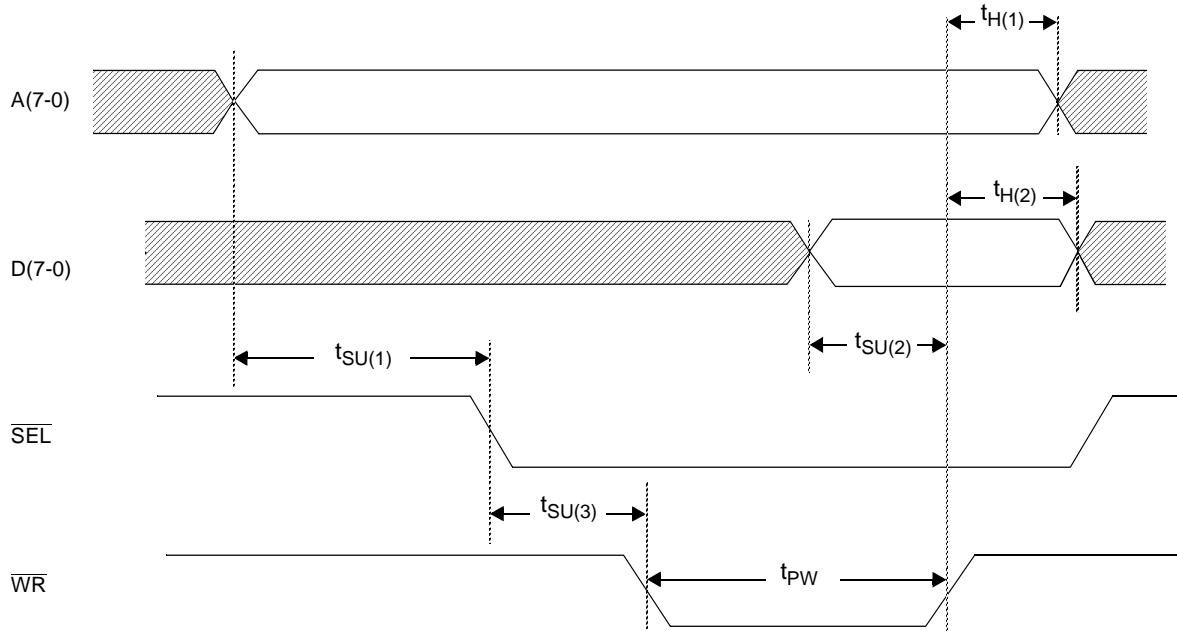
Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	0.0			ns
A(7-0) address setup time before $\overline{SEL}\downarrow$	$t_{SU(1)}$	20			ns
D(7-0) data valid setup time before $\overline{WR}\uparrow$	$t_{SU(2)}$	20			ns
D(7-0) data hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	5			ns
$\overline{SEL}\downarrow$ setup time before $\overline{WR}\downarrow$	$t_{SU(3)}$	10			ns
$\overline{WR}$ pulse width	t_{PW}	80		212,000	ns

Notes:

1. The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate. The RDY/DTACK output lead is always driven high when the $\overline{SEL}$ lead is low, otherwise it is tri-stated, which corresponds to the behavior of the M13E device.

2. The $\overline{SEL}$ lead must be brought high for 2 transmit clock cycles before the start of a new write cycle.

Figure 16. Microprocessor Read Cycle Timing - Motorola Interface
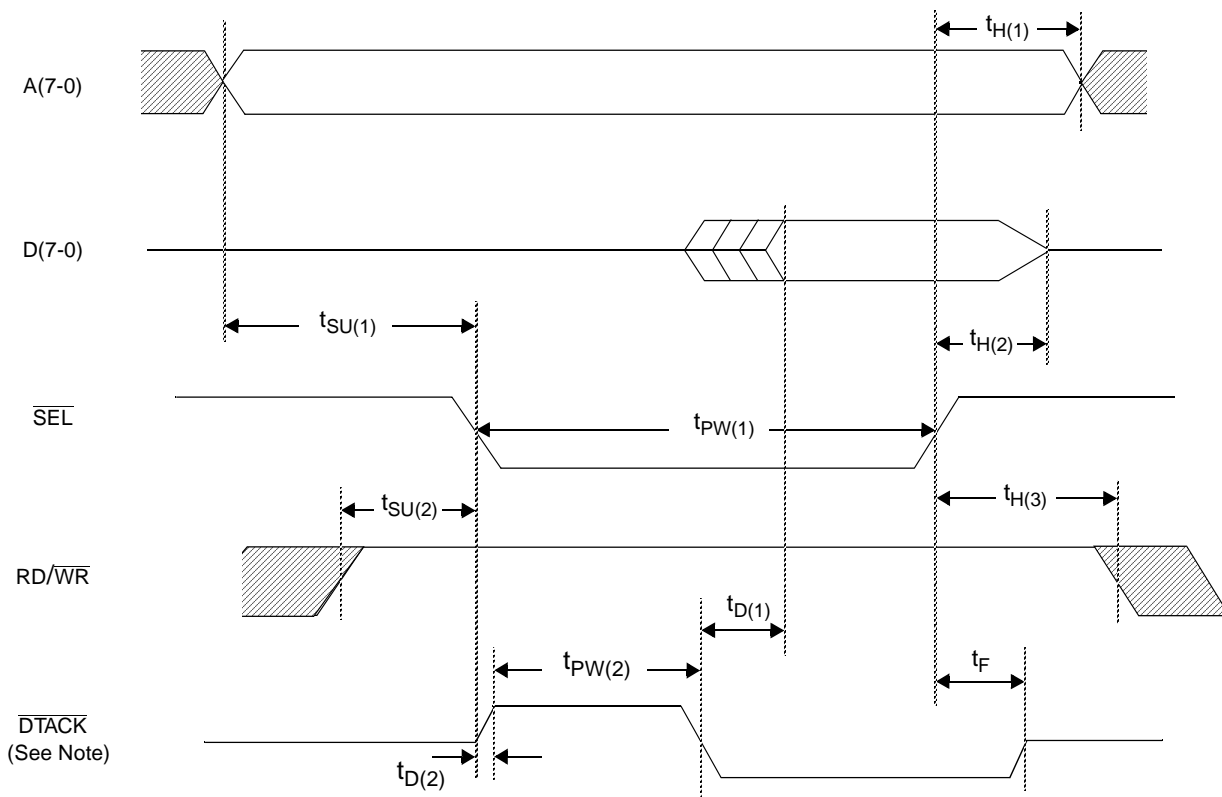
Note: The $\overline{DTACK}$ signal lead is tri-stated when $\overline{SEL}$ is high.

Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
A(7-0) address valid setup time before $\overline{SEL}\downarrow$	$t_{SU(1)}$	20			ns
D(7-0) data valid delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$		16	21	ns
D(7-0) data hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$			42	ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	60		212,000	ns
RD/$\overline{WR}\uparrow$ setup time before $\overline{SEL}\downarrow$	$t_{SU(2)}$	20			ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			60	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0.0		100	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			20	ns

Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate. The $\overline{DTACK}$ signal lead has the same functional timing as the M13E device when the $\overline{M13X}$ lead is high.

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Figure 17. Microprocessor Write Cycle Timing - Motorola Interface

Note: The $\overline{\text{DTACK}}$ signal lead is tri-stated when $\overline{\text{SEL}}$ is high.

Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{\text{SEL}}\uparrow$	$t_{H(1)}$	0.0			ns
A(7-0) address valid setup time before $\overline{\text{SEL}}\downarrow$	$t_{SU(1)}$	20			ns
D(7-0) data valid setup time before $\overline{\text{SEL}}\uparrow$	$t_{SU(2)}$	10			ns
D(7-0) data hold time after $\overline{\text{SEL}}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{\text{SEL}}$ pulse width	$t_{PW(1)}$	60		212,000	ns
RD/$\overline{\text{WR}}\downarrow$ setup time before $\overline{\text{SEL}}\downarrow$	$t_{SU(3)}$	20			ns
RD/$\overline{\text{WR}}\uparrow$ hold time after $\overline{\text{SEL}}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{\text{DTACK}}\uparrow$ delay after $\overline{\text{SEL}}\downarrow$	t_D			60	ns
$\overline{\text{DTACK}}$ pulse width	$t_{PW(2)}$			100	ns
$\overline{\text{DTACK}}$ float time after $\overline{\text{SEL}}\uparrow$	t_F			20	ns

Note: The transmit clock (XCK) or receive clock (DS3CR) must be present for the microprocessor bus interface to operate.
The $\overline{\text{DTACK}}$ signal lead has the same functional timing as the M13E device when the $\overline{\text{M13X}}$ lead is high.

Figure 18. Boundary Scan Timing
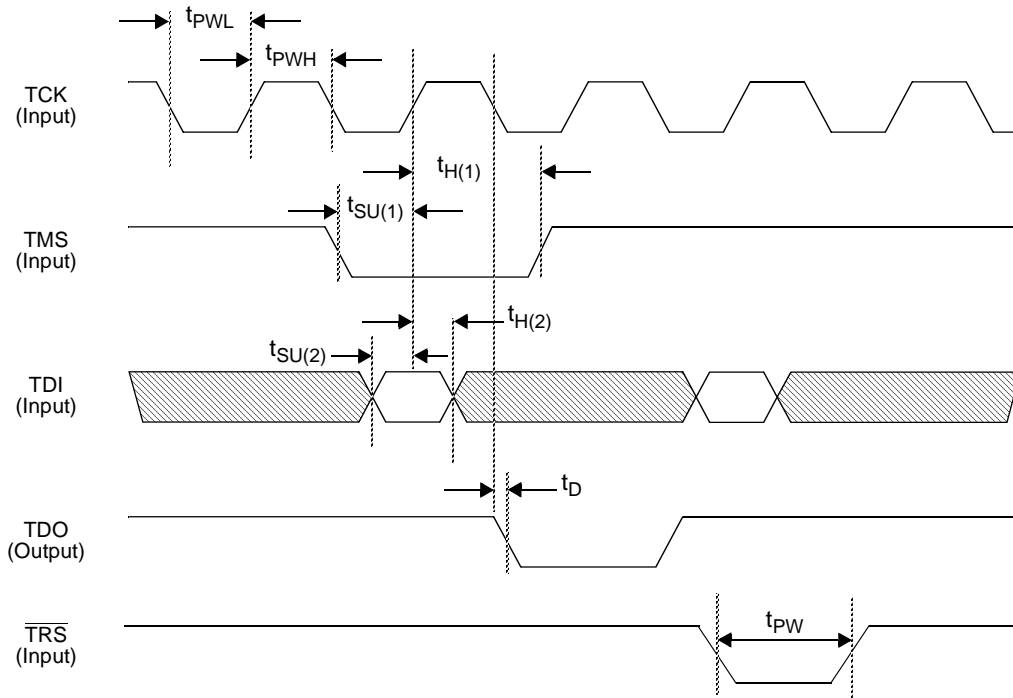
Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time before TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time before TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	3.0	-	ns
TDO delay from TCK↓	t_D	-	10	ns
$\overline{TRS}$ pulse width	t_{PW}	100	-	ns

OPERATION

The sections below contain descriptions of the M13X features. In the M13X device, the counters, interrupt request bits, interrupt mask bits, new control bits, and PMDL FIFO interface will be located at addresses 25H-3FH.

$\overline{M13X}$ LEAD

In order to maintain backwards compatibility with the M13E device, a control lead with an internal pull-up, $\overline{M13X}$, has been added. When this lead is set to high, or left floating, all of the M13X functions contained in address locations 25H-3FH are disabled. This means that:

- The PMDL (Path Maintenance Data Link) C-bits are inserted and extracted solely through the external C-bit interfaces (in C-bit Parity format mode) or by the internal stuffing logic (in M13 format mode).
- The internal dejitter buffers (DJBs) are bypassed.
- The external address straps S5-S7 operate as in the M13E device.
- Only the registers defined by the settings of the µP0 and µP1 leads and straps S5-S7 are accessible. Any reads from addresses outside of those ranges cause the microprocessor interface of the M13X to remain tri-stated. Any writes to locations 25H-3FH will not have any effect on device operation. Furthermore, when the µP0 and µP1 leads are both set to high, registers 20H-3FH are not accessible for read or write operations.
- All counters are 8 bits long, clear when read, and saturate when a count of FFH is reached.
- The $\overline{TXFRM}$ lead is operational.
- NEW bit will be set under the conditions that caused the NEW bit to be set in the M13E device. Namely, the NEW bit becomes set when any five consecutive and identical FEAC messages are received. The NEW bit will continually be reasserted if it is read and cleared when a continuous constant FEAC message is received.

When the $\overline{M13X}$ lead is set to low:

- The bits in registers 25H-3FH can be used to control, enable/disable, and monitor the M13X functions.
- The address strap S5 is ignored.
- Address straps S6 and S7 are enabled to allow the M13X to be mapped to address ranges 00H-3FH, 40H-7FH, 80H-BFH, or C0H-FFH. When the M13X is mapped to an address range, all accesses to addresses outside of that range are handled by the M13X as if the $\overline{SEL}$ chip-select input lead is high. That is, all read operations cause the microprocessor bus to be tri-stated and write operations will not have any effect upon any register. Furthermore, when lead µP1 is high and µP0 is low, the multiplexed mode of operation is selected, but access to all registers (00H-3FH) is provided. Setting both µP1 and µP0 high is not allowed.
- The counters become 16 bits in length, clear when read, and saturate[1] when a count of FFFFH is reached. When the low byte of a 16-bit counter is read, the high byte is simultaneously written to a common high byte register location (3EH). So, in order to read a 16-bit counter, the counter register is read first to get the low byte, then the common high byte register is read to get the high byte.
- The $\overline{TXFRM}$ lead is operational.
- NEW bit in register 1DH does not become set to one again after it is cleared when a continuous constant FEAC message is received.

Regardless of the setting of the $\overline{M13X}$ lead, the M13XID0 bit (register 10H, bit 7) bit will always be set to 0. The

1. Saturate, as used throughout this document when referring to a counter, means that a counter stops at its maximum count and does not roll over to zero when the next count event occurs.

M13XID0 bit is used by external software to determine if the device being accessed contains an M13E or an M13X die. The end user would use this bit as follows before the device is configured:

- Register 10H is written with 00H
- The end user verifies that 10H contains 00H
- Register 10H is written with 80H
- The end user reads 10H again. If it is 00H, then the device contains an M13X die. If 80H is read back, then the device contains an M13E die.
- As an additional check to ensure that the microprocessor interface is working, the end user can verify that bit 7 of register 11H can be written with a 1 and a 0. This bit does not do anything in either device, it is just a read/write bit.

RESETS

An active low hardware reset signal lead, $\overline{\text{HRESET}}$, is provided to reset the M13X device from an external source. The operation of this lead is also asynchronous. When this lead is asserted low the following functions occur:

- Reset registers 00H, 02H-14H, and 16H-3FH to 00H.
- Reset register 01H to 01H.
- Reset register 15H to 7FH.
- Perform the same reset functions as the software reset of register 1FH.
- Reset all of the device to a known state.

Please note that the hardware reset does not have any effect on the boundary scan TAP controller.

Figure 19 shows the functional architecture of the resets in the M13X device. Please note that this diagram represents functionality and not necessarily implementation.
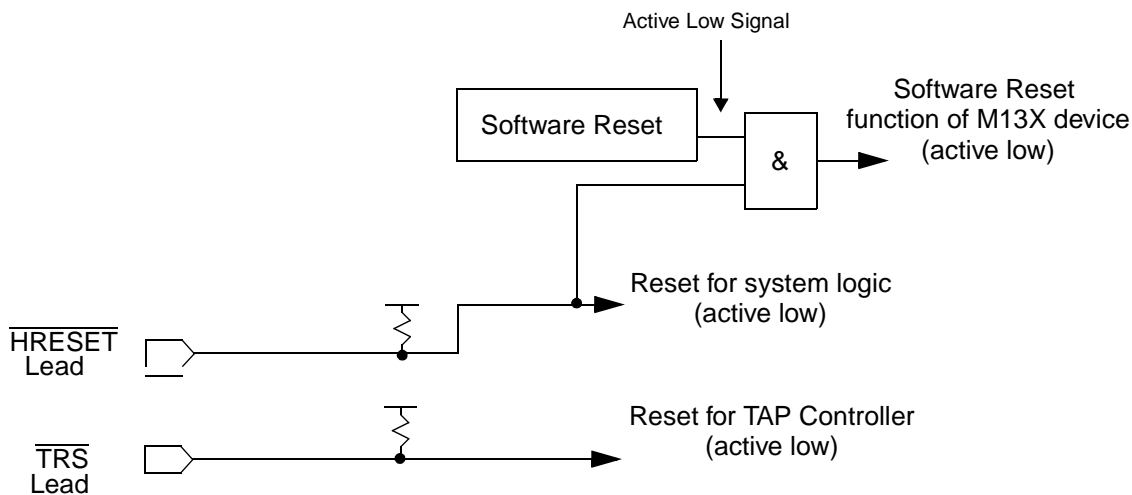
Note: Low corresponds to logic 0 in this diagram.

Figure 19. M13X Reset Structure

INTEGRATED DJB DEVICES

The dejitter buffer (DJB) is a TranSwitch circuit design that takes in jittered DS1s from a DS3 to DS1 demux process and smooths out the DS1s. The M13X device contains 28 of these DJBs. The option to bypass the DJBs through a control bit, DJB, is provided when the $\overline{M13X}$ lead is low. When $\overline{M13X}$ is high, the DJBs are unconditionally bypassed.

The DJB control bit is located at bit 7 of register 3DH. When $\overline{M13X}$ is low the DJB control bit operates as follows:

- DJB = 0. The DJBs are bypassed.
- DJB = 1. The DJBs are enabled and the 28 receive DS1s are dejittered.

The DJBs are located in the M13X device such that when they are enabled (i.e., DJB = 1 and $\overline{M13X}$ is low), the receive DS1 channels that are looped back are also dejittered. The XCK signal is normally used to operate the DJBs, therefore it needs to be stable and clean. In the event that the XCK clock is lost (i.e., T3CKF = 1), the DS3CR clock is automatically substituted in place of the XCK clock. Each DJB has an automatic self-reset function that allows individual DJBs to be reset (i.e., only the DJBs that need to be reset are reset, while the others operate normally) upon DJB FIFO underflow/overflow. However, when the 44.736 MHz reference clock to the M13X is switched from XCK to DS3CR or vice versa, a manual reset via the software reset register can be performed via software control. The following conditions activate the DJB reset:

- Software reset activated
- Hardware reset activated
- FIFO overflow or underflow (in this case, the reset is performed automatically for the individual DJB that has underflowed or overflowed)

Note that, when in loop timing mode (LPTIME = 1), the transmit clock (in this case the DS3CR signal) is used as the 44.736 MHz reference clock for the DJBs. The DS3 reference clock frequency tolerance needs to be within ± 20 ppm inclusive. The DS1 signals that are embedded in the demuxed DS3 signal originated at a mux somewhere else in the system. The original frequency of these DS1s needs to be within ± 130 ppm of the nominal frequency.

The M13X meets and exceeds the jitter requirements for all possible combinations of DS3 and DS1 clock offsets indicated below:

- DS3 clock offset: +/- 20 ppm ([GR-499] Table 9-16 Line-rate accuracy parameter)
- TX DS1 clock offset: +/- 130 ppm ([GR-499] R9-64 section 9.3.2)
- RX DS1 clock offset: +/- 32 ppm ([GR-499] Table 9-13 Line-rate accuracy parameter). This parameter must always be met when the line rate of the channelized DS1 signal being demultiplexed is within +/- 32 ppm.

The M13X meets and exceeds the timing jitter requirements specified in [GR-499] for:

- Tolerance ([GR-499] section 7.3.1)
- Transfer ([GR-499] section 7.3.2)
- Generation ([GR-499] section 7.3.3)
- Enhancement ([GR-499] section 7.3.4)

JITTER TOLERANCE

Input jitter tolerance is defined in [GR-499] section 7.3.1 as:

"The minimum amplitude of sinusoidal jitter at a given frequency that, when modulating the signal at an equipment input port, results in more than 2 errored seconds in a 30-second measurement interval."

In accordance with the above, the M13X was tested in all the channelized T1 signals during a 30-second measurement interval when the jitter mask indicated below was applied to the TX DS1 signals when the TX DS3 clock (XCK or DS3CR) and the TX DS1 input clocks were varied over their line rate accuracy specified above.[1] This requirement was also met when Loop Timing mode was enabled and the maximum amount of tolerable jitter applied to the DS3CR signal (i.e. the TX clock). The M13X tolerated more jitter than is indicated in the GR-499 mask requirements, as shown below.

The M13X was tested in the T3 and channelized T1/T2[2] signals during a 30-second measurement interval when the jitter mask indicated below was applied to the RX DS3 signal when the RX DS3 clock (DS3CR) and the channelized DS1 input clocks were varied over their line rate accuracy specified above. The M13X tolerated more jitter than is indicated in the GR-499 mask requirements, as shown in Figures 20 and 21.

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1. When verifying DS1 jitter tolerance, it is acceptable to loop back the DS3 signal and measure the errors that occur on the demultiplexed DS1 signals. The DJBs should be enabled during such a test to ensure that they do not drop data.

2. It is sufficient to only check the RX DS1s for errors, however a more complete, but not required, check should include all of the signals.

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Figure graph: Input Jitter Amplitude (UIpp) vs Jitter Frequency (Hz)

- Measured for M13X
- slope = -28.22 dB/decade
- DS1 Jitter Tolerance Mask to GR-499-CORE

Jitter Frequency (Hz)
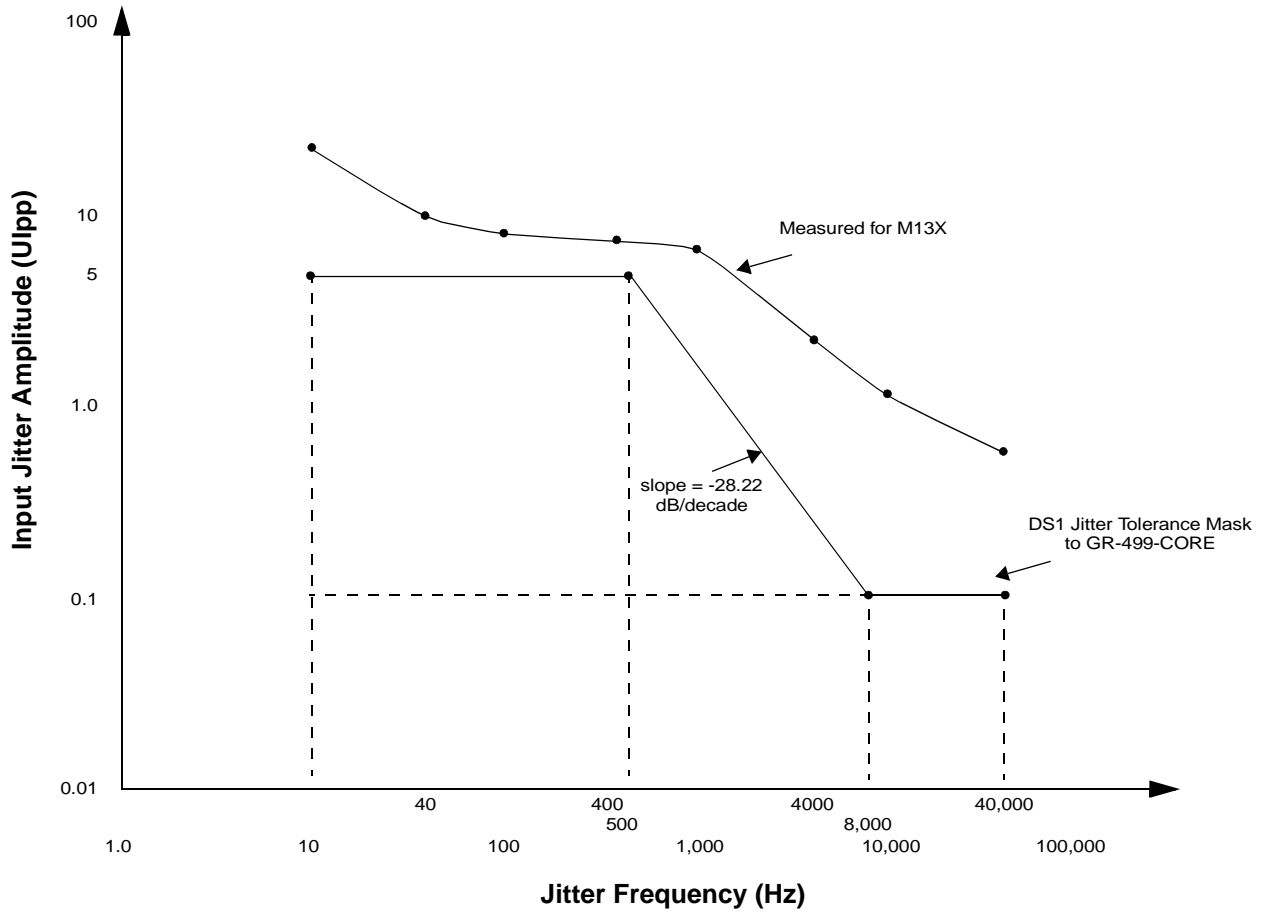
Jitter Frequency (Hz)	Input Jitter Amplitude (UIpp)
10	18.564
40	9.814
100	7.314
400	6.064
1000	5.861
4000	2.423
10000	1.134
40000	0.556

Figure 20. DS1 Input Jitter Tolerance

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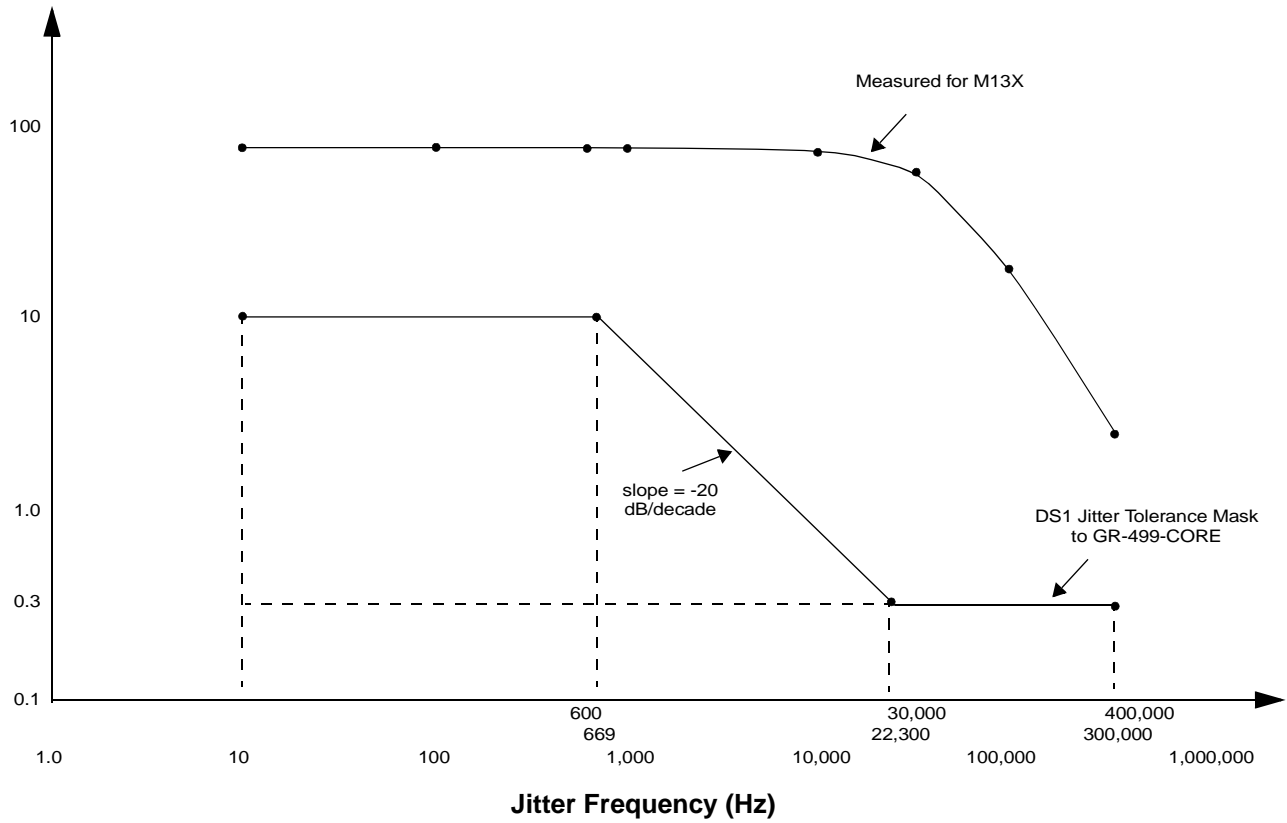
Jitter Frequency (Hz)	Input Jitter Amplitude (Ulpp)
10	<64
100	<64
600	<64
1,000	<64
10,000	<64
30,000	59.438
100,000	17.139
400,000	2.374

Figure 21. DS3 Input Jitter Tolerance

JITTER TRANSFER

Jitter transfer requirements are defined in [GR-499] section 7.3.2 for DS3 to DS1 and also for DS1 to DS3 to DS1 interfaces. The jitter transfer functions listed below shall be met for all DS1 and DS3 frequency offsets, and DJB reference clock offsets; the actual performance of the part at typical clock frequency offsets is super-imposed.

The jitter transfer masks shown in Figures 22 and 23 show the maximum allowable gain in the jitter over a specified range of frequencies going from one port to another.

Note: Only at 15 KHz, the M13X exceeds the Jitter Transfer Mask Limits; and that is because the generated jitter at those frequencies is high compared to the 0.3 UI input jitter applied. The generated jitter is well within the 1.0 UI spec at 15 KHz. The GR-499-CORE section 7.3.2 states that at such frequencies, the jitter transfer cannot be measured.
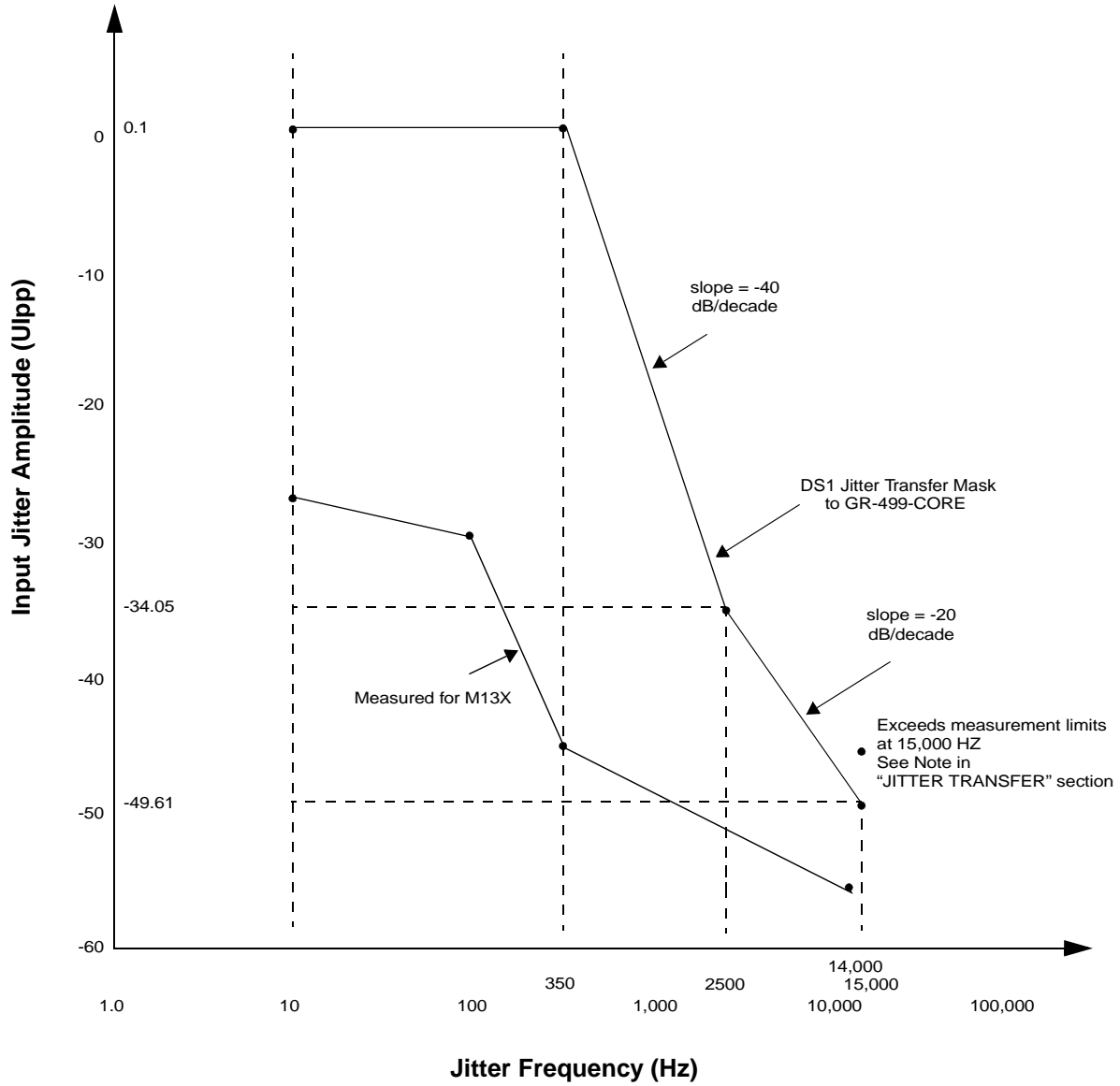
Jitter Frequency (Hz)	Jitter Gain (dB)
10	-25.11
100	-28.42
1,000	-45.18
14,000	-56.40
15,000	-46.07

Figure 22. DS3 to DS1 Interface Jitter Transfer Limits

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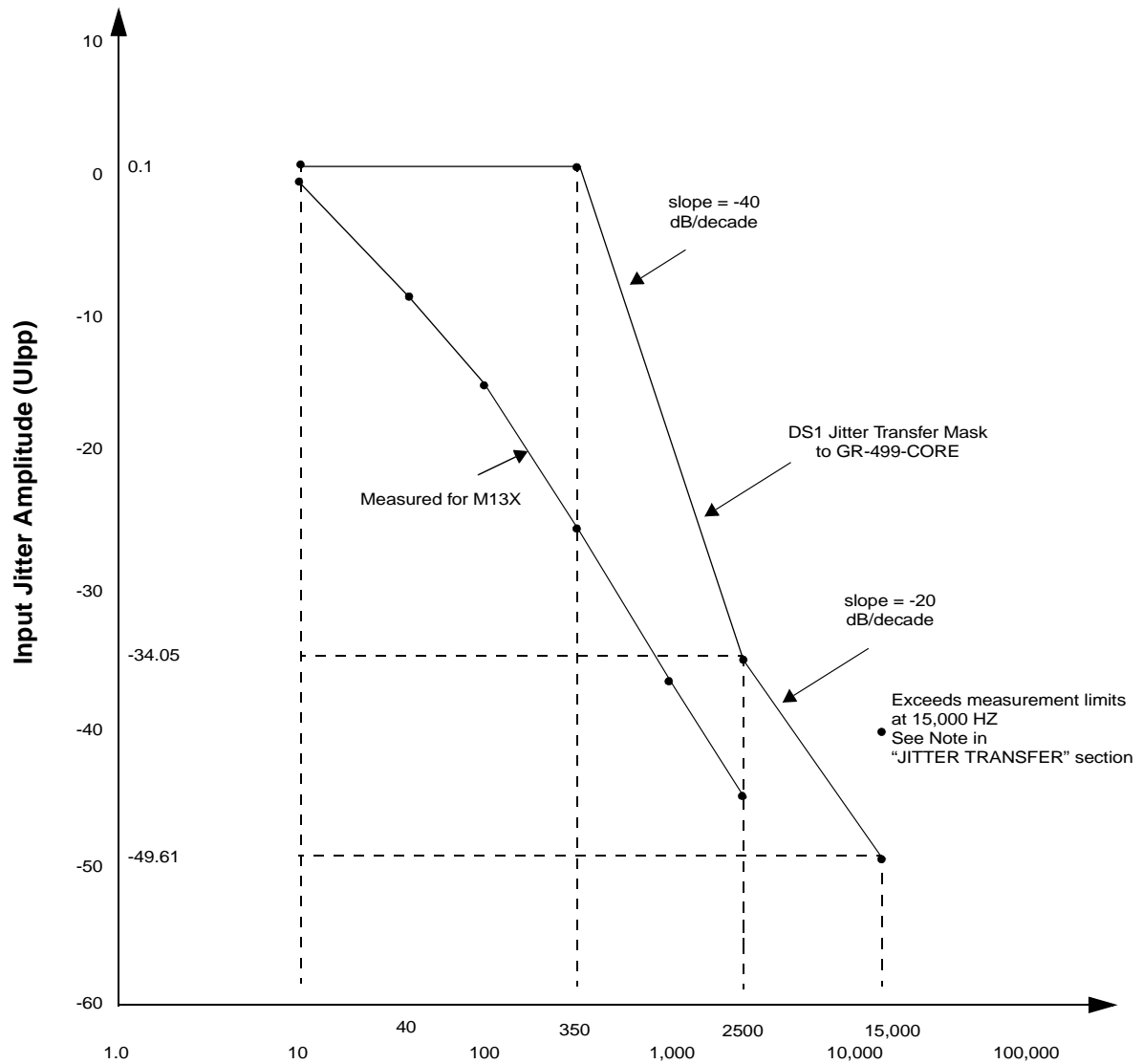
Jitter Frequency (Hz)

Jitter Frequency (Hz)	Jitter Gain (dB)
10	0.07
40	-8.16
100	-15.72
350	-27.42
1,000	-37.00
2,500	-44.71
15,000	-40.46

Figure 23. DS1 to DS1 Jitter Transfer Limits

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JITTER GENERATION

In the absence of input jitter on any clock applied to the M13X device, the jitter generated at the RX DS1 output (with the DJB function enabled) shall be less than 0.3 UIrms and also less than 1.0 UIpp over the jitter frequencies of 10 Hz - 40 KHz ([GR-499] R7-7 section 7.3.3 and Table 7-1) and over all of the DS1 and DS3 clock offsets. This requirement applies only to a multiplexer demultiplexer pair.

Jitter generation criteria for the DS3 interface is not defined at this time. As a goal, the jitter at the TX DS3 output of a ARTE/M13X pair is required to be less than 5 UIpp over a jitter frequency range of 10Hz - 400 KHz and 0.1 UIpp over a jitter frequency range of 30 KHz - 400 KHz.

JITTER ENHANCEMENT

The DS1 jitter output at an RX DS1 of the M13X is less than 5.0 UIpp over a jitter frequency range of 10 KHz - 40 KHz, after that DS1 signal went through 12 (or more) M13X multiplexer/demultiplexer pairs. This requirement is met when the 1st DS1 signal has 4.0 UI applied to it over a jitter frequency range of 10 Hz - 350 Hz. This requirement does not need to be met when the DJBs are bypassed but must be met when they are enabled. Also, no bit errors occur.

RESIDUAL JITTER

When the DJBs are enabled and the demultiplexed DS1 signals do not have any jitter on them, the DS1 jitter output of the M13X is about 0.30 UIpp and 0.038 UIrms over a 10Hz - 40 KHz jitter frequency range and about 0.028 UIpp and 0.014 UIrms over an 8 KHz - 40 KHz jitter frequency range for all DS1 and DS3 clock offset frequencies.

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INTERRUPTS

A set of interrupt request bits and corresponding mask bits is provided in the M13X. An interrupt request bit is a bit that latches to a 1 when a certain condition occurs and can cause an interrupt to be signaled on an external interrupt request lead (INT/$\overline{\text{IRQ}}$) if the corresponding interrupt request mask bit is also set to a 1. An interrupt request bit will remain set to a 1 even when the condition that caused it to become set is removed. An interrupt request bit can be cleared by reading it. Two control bits, RISE and FALL, are used to control the conditions for setting the non-PMDL related interrupt request bits. When RISE = 1, the interrupt request bits are set on the entrance of an alarm/condition. When FALL = 1, the interrupt request bits are set on the exit of an alarm/condition. When RISE and FALL are both set to 1, the interrupt request bits are set on both the entrance and exit of an alarm/condition. When RISE and FALL are both set to 0, the interrupt request bits are disabled. Note that the RISE and FALL bits do not affect the PMDL interrupt request bits in register 2CH. These bits are significant only when set on the entrance of a condition and therefore only become set on the entrance of their corresponding condition.

It is important to note that the interrupt request bits are set by their real-time counterparts, and not from other latched bits. For example, the interrupt request bit for the R3LOS alarm is not set by the latched R3LOS bit in register 16H but is set by the real-time R3LOS bit in register 00H.

Interrupts need to be serviced within a specific period of time after they are signaled by the INT/$\overline{\text{IRQ}}$ lead. The table below indicates the time interval within which the interrupt request bits need to be read and processed.

Register Address (Hex)	Description
25	The IRLBn and IRLBALL bits should be accessed within 131 µs.
26	The IRLBn and IRLBDS3 bits should be accessed within 131 µs.
27	The IRLBn bits should be accessed within 131 µs.
28	This register should be read within 7.6 µs to ensure that the IRSEF bit is read before it can change.
29	This register should be read within 7.6 µs to ensure that the DS3 status bits are read before they can change.
2A	This register should be read within 26 µs to ensure that the IRDS2OOFn bits are read before they can change.
2B	Once a counter saturates, it must be read before the next count comes in to ensure that no counts are lost. The worst case condition would occur for the F and M bit error counters (register 04H in M13 format mode) and register 1BH. In this case this register and the DS3 F-bit and M-bit counter would need to be read within 1.9 µs. Since the M13X provides 16-bit wide counters (when $\overline{\text{M13X}}$ is low) the counters do not have to be read very often to ensure that they do not saturate. Reading the 16-bit counters in the M13X once a second is sufficient to ensure that they will not saturate.
2C	Once an interrupt request from one of the PMDL controllers is received it is recommended that this register, the RX PMDL MESSAGE LENGTH register (39H), the RX PMDL FIFO DEPTH register (3AH), and at least one byte from the RX PMDL FIFO interface register (38H) are read within 212 µs before they can be updated by the next PMDL byte.

PMDL OPERATION

The terminal-to-terminal path maintenance data link (PMDL) is a 28.2 kbit/s channel, which is available in the C-bit Parity format mode, and is used to communicate DS3 path identification, DS3 signal identification, and DS3 test signal identification between terminals. The PMDL channel is carried in the C13, C14, and C15 DS3 C-bits and uses an HDLC protocol as defined in ITU-T Recommendation Q.921 (3/93).

The HDLC message frame is composed of four parts: an opening flag, the message (which consists of 79 bytes), a two-byte FCS-16 frame check sequence, and a closing flag, as shown in 24 below.

Bit	8	7	6	5	4	3	2	1
Opening Flag	0	1	1	1	1	1	1	0
Message	Address and Control Information (79 bytes)							
FCS-16	2^8							2^{15}
	2^0							2^7
Closing Flag	0	1	1	1	1	1	1	0

Figure 24. HDLC Format

The bit numbering convention indicated in [Q.921] sections 2.8.2 and 2.8.3 is followed in Figure 24. The PMDL block (or HDLC Controller) performs the following functions:

- Zero bit stuffing/destuffing (11111 to 111110 /111110 to 11111) ([Q.921] section 2.6)
- ITU-T FCS-16 generation/checking (16-bit sequence) ([Q.921] section 2.7)
- Flag generation/detection (01111110) ([Q.921] section 2.2)
- Abort generation/detection (01111111...) ([Q.921] section 2.10)
- Start of frame detection ([Q.921] section 2.2)
- End of frame detection ([Q.921] section 2.2)
- FIFO overflow and underflow
- Invalid frame detection and discard ([Q.921] section 2.9).

Bit 1 is the least significant bit and is the first bit transmitted/received. The opening and closing flags are represented by a single, unique 8-bit character defined as 01111110, which contains six contiguous ones. A two-byte FCS-16 frame check sequence is computed across the contents of the message (after the opening flag), and appended to the end of the message. The polynomial for the FCS is $x^{16}+x^{12}+x^5+1$ as specified in [Q.921] section 2.7. To avoid the occurrence of a false flag within the transmit data stream, a 0 is inserted (stuffed) after each string of five contiguous ones between the opening and closing flags. The time between consecutive frames is filled with one or more flags.

In the receive direction, the HDLC controller frames to the flag characters to determine the byte boundary and the start of the data. All flags are discarded and destuffing is performed on the data. Destuffing is the process of replacing any 111110 patterns detected between the opening and closing flags with 11111. Reception of more than six contiguous ones before destuffing is interpreted as a frame abort sequence. When an abort sequence is received, the remainder of the current frame is ignored and the received portion should be discarded by the end user as an invalid frame. When two or more frames occur in sequence, they may share the boundary flag between them (i.e., the closing flag of the first frame can serve as the opening flag of the next frame) ([Q.921] section 2.2). The M13X is able to successfully delineate HDLC-encapsulated PMDL messages in this case.

An 80-byte PMDL FIFO is provided in the transmit direction to allow at least one complete message to be stored for processing. A 159-byte PMDL FIFO is provided in the receive direction, which permits at least two

ANSI T1.107 LAPD messages to be received. Interrupts and status information are provided to facilitate FIFO servicing by the microprocessor.

The HDLC receiver is enabled when a 1 is written to control bit EHR (bit 4) in register 3DH. When enabled, the receive PMDL C-bits (C13, C14, and C15) are extracted from the receive DS3 stream. The flag sequence is checked to determine the byte boundary. After the octet boundary is established, the first non-flag octet signifies the start of the information field. At this point, the HDLC receiver will remove the stuffed 0 bits and place the message contents, aligned to octet boundaries, into the 159-byte receive PMDL FIFO. It is important to note that the first bit received is the least significant bit and goes into bit location 0^1 of the octet.[2] The HDLC controller will check the FCS to ensure that it is correct. The received FCS is not stored in the FIFO and is discarded after being checked. Only the de-stuffed information between the opening and closing flags is written to the receive PMDL FIFO. Please note that receive PMDL FIFO overflow does not necessarily result in an FCS error since the FCS is checked before data is written into the receive PMDL FIFO. If the FCS check fails, then the RX FCS ERROR Counter at address 3BH increments and the IRRHIS(2-0) bits in register 2CH are set to 011 to signal that an FCS error has occurred. The RX FCS ERROR Counter is a read-only 16-bit counter that clears on read. FCS Error Counts are not lost during a read. If an abort sequence is detected (i.e., an octet that contains more than 6 consecutive 1s is detected), only the information field received up to that point is written to the receive PMDL FIFO. Furthermore, the RX ABORT Counter at register 3CH increments, and the IRRHIS(2-0) bits in register 2CH are set to 100 to signal that an abort has occurred. The RX ABORT Counter is a 16-bit read only counter that clears on read. ABORT counts are not lost during a read of this counter. The RX PMDL FIFO DEPTH and RX PMDL MESSAGE LENGTH registers, at 3AH and 39H, are also updated accordingly, as described in the paragraphs below. The receive DS3 C-bit interface operation is not affected by the setting of the EHR control bit. When EHR = 0, the receive PMDL controller is disabled, and no interrupt requests are generated.

The receive PMDL FIFO is monitored for fill level, with maskable interrupts provided. Bits IRRXFS1 and IRRXFS0 (bits 4 and 3) in register 2CH indicate when the receive PMDL FIFO is equal to or greater than half full, full, and overflowed. An interrupt may also be activated at the end of the message, or when the FIFO is half full, using the RHIE control bit (bit 5) in register 3DH to control the conditions for which interrupt request bits IRRHIS(2-0) (bits 7 - 5) in register 2CH change. If it is desired to signal an interrupt at the end of a message, the RHIE control bit can be set to 0. Then the HDLC controller will generate an interrupt only on the completion of the message. If mask bits MIRRHIS(2-0) (bits 7 - 5 in register 35H) are set to 110, an interrupt will occur when IRRHIS(2-0) = X1X or 1XX; IRRHIS(2-0) will also hold the latched value. The controller will generate an interrupt when the FIFO is half filled by setting $RHIE^3$ = 1; mask bits MIRRHIS(2-0) should be set to 110, but now the interrupt based on IRRHIS(2-0) = 010 will occur both at the end of message and when the FIFO reaches half full. This same function may be accomplished by leaving RHIE = 0 and by monitoring the FIFO fill level using status bits IRRXFS1 and IRRXFS0 to detect FIFO fullness. To generate an interrupt from the IRRXFS1 and IRRXFS0 interrupt request bits, mask bits MIRRXFS1 and MIRRXFS0 (bits 4 and 3) in register 35H should be set to 11; when the receive PMDL FIFO is equal to or more than half full, interrupt request bits IRRXFS1 and IRRXFS0 (bits 4 and 3) in register 2CH will be set to 01 and an interrupt will be generated.

The RX PMDL FIFO DEPTH register at address 3AH provides the number of bytes presently stored in the receive FIFO. Bits IRRHIS(2-0) (bits 7-5 in register 2CH) provide message status and error indications. The receive PMDL controller will generate a maskable interrupt for start of message detected, valid message received, FCS in error, message aborted, and invalid frame received. The message bytes are read by the microprocessor from the RX PMDL FIFO at register 38H. Bit 0 corresponds to the first bit received in a byte.

To accommodate back-to-back messages, a RX PMDL MESSAGE LENGTH register is provided at address 39H, which is loaded with the length of the received message, in bytes, at the end of every message (valid

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1. TranSwitch bit numbering format is used here. Bits are ordered 7-0 (most significant bit - least significant bit).

2. CAUTION: The first bit transmitted/received in the HDLC protocol is the least significant bit. See sections 2.8.1 and 2.8.2 in [Q.921]. Please also note that in [Q.921] bits are numbered 8-1 (most significant bit-least significant bit) instead of 1-8 (most significant bit-least significant bit) as in some other documents.

3. This setting of RHIE is used when the message is expected to be longer than 159 bytes.

received, aborted, received with bad FCS, or an invalid frame was received). When an interrupt occurs indicating a message has been received, the RX PMDL MESSAGE LENGTH register should be read. The message length along with message status may be queued for processing later. The value in the RX PMDL FIFO DEPTH register is not reset at the end of a message. When initializing the HDLC controller, the receive PMDL FIFO must be read repeatedly until the depth value in the RX PMDL FIFO DEPTH register is zero. It should be noted that messages with bad FCS or messages that were aborted must also be cleared from the receive PMDL FIFO by the end user.

Invalid frames are detected and discarded. [Q.921] section 2.9 identifies and defines six different situations that can be considered an invalid frame:

   a. A frame that is not properly bounded by two flags (i.e., a frame that violates a maximum or minimum length). The M13X will allow any length frame to be received, therefore it will be up to the end user's software to determine if the received frame is too long.

   b. There are fewer than 6 octets between flags of frames that contain sequence numbers and fewer than five octets between flags of frames that do not contain sequence numbers (for the case of the M13X, unnumbered sequences are used, see Figure 26 in [T1.107] and sections 3.4 and 3.4.3 in [Q.921], therefore the 5 octet requirement applies to the M13X).

   c. The frame does not consist of an integral number of octets prior to bit insertion or following zero bit extraction.

   d. The frame contains a frame check sequence error.

   e. The frame contains a single octet address field.

   f. The frame contains a service access point identifier ([Q.921] section 3.3.3) which is not supported by the receiver.

Items a-f below indicate how the requirements in items a-f directly above are implemented in the M13X:

   a. No hardware support is provided for detecting if received frames are too long. The M13X can accept frames of any length. Software can determine that the frame is too long and can read it out of the FIFO and then chose to discard the data.

   b. When a frame contains 4 or fewer octets, after destuffing, between its opening and closing flags:
   - The IRRHIS(2-0) interrupt request bits (bits 7-5 of register 2CH) are set to 111.
   - The frame is written to the receive PMDL FIFO.
   - The RX PMDL FIFO DEPTH register indicates the correct depth of the receive PMDL FIFO.
   - The RX PMDL MESSAGE LENGTH register indicates the correct message length.
   - An FCS error is not counted or declared.

   c. When a receive[1] frame does not consist of an integral number of octets after the destuffing process:
   - The IRRHIS(2-0) interrupt request bits (bits 7-5 of register 2CH) are set to 111.
   - The frame is written to the receive PMDL FIFO, except for the partial byte.
   - The RX PMDL FIFO DEPTH register indicates the correct depth of the receive PMDL FIFO.
   - The RX PMDL MESSAGE LENGTH register indicates the correct message length.
   - An FCS error is not counted or declared.

   d. When a receive frame contains a frame check sequence error:
   - The IRRHIS(2-0) interrupt request bits (bits 7-5 of register 2CH) are set to 011.

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1. Transmit frames in the M13X are exempt from checking, since the transmit PMDL data are written into the transmit PMDL FIFO as octets. Also, it is not expected that the transmit PMDL message stop transmitting on a non-octet boundary. Therefore all transmit PMDL messages will default to an integral number of octets in length, before stuffing.

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- The frame is written to the receive PMDL FIFO.
- The RX PMDL FIFO DEPTH register indicates the correct depth of the receive PMDL FIFO.
- The RX PMDL MESSAGE LENGTH register indicates the correct message length.
- The RX FCS ERROR Counter increments by 1.

e. No hardware support is provided for receive frames that have a single octet address field. This type of frame is handled as a normal frame. User software can determine that the frame has a single octet address field by reading it out of the FIFO and then choose to discard the data.

f. No hardware support is provided for receive frames that have an invalid service point access identifier. This type of frame is handled as a normal frame. Software can determine that the frame has an invalid service point access identifier by reading it out of the FIFO and then choose to discard the data.

The transmit PMDL controller is disabled when a 0 is written to control bit EHT (bit 0) in register 3DH or when a high is applied to the $\overline{\text{M13X}}$ lead or it is left floating. When disabled, the PMDL C-bits are sourced from either the external DS3 C-bit interface when M13MODE = 0 (bit 0 register 02H) or from internal stuffing logic when M13MODE = 1. The HDLC transmitter is enabled when a 1 is written to control bit EHT while a low is applied to the $\overline{\text{M13X}}$ lead. When enabled, the transmit PMDL controller will transmit flags until data is placed in the transmit FIFO. Up to 80 bytes can be placed in the transmit PMDL FIFO at once, but only 79 bytes are required. The message bytes must be written into the transmit PMDL FIFO by writing into the TX PMDL FIFO register at 37H. Bit 0 corresponds to the first bit transmitted. The transmit bytes are read from the transmit PMDL FIFO, a 16-bit FCS is computed until the end of message is detected, and zero insertion (stuffing) is performed over the message and FCS as needed. Please note that the stuffing function is performed on all of the bytes between the opening and closing flags including the FCS. The FCS is calculated over the unstuffed raw data between, but not including, the last bit in the opening flag and the first bit of the FCS. When the last byte of the message is written into the FIFO, the microprocessor must set the end of message status bit EOM (bit 2) in register 3DH. This allows the end of the message to be identified to the internal logic, so that it knows where to put the FCS. The computed 16-bit FCS will be appended to the end of the message followed by at least one flag before another message is transmitted. When the transmit PMDL FIFO is emptied without setting the EOM bit, the FIFO will set an underflow indication value of 11 in interrupt request bits IRTXFS1 and IRTXFS0 (bits 2 and 1) in register 2CH, and an abort character will be transmitted, thereby terminating the message. If the transmit PMDL FIFO is emptied after the EOM bit is set, then the interrupt request bits IRTXFS(1-0) are not set, the FCS is appended to the end of the message as appropriate and then flags are transmitted until another message is transmitted.

The transmit HDLC controller provides interrupt request bits and corresponding interrupt request mask bits related to the transmit PMDL FIFO status. Information such as underflow and fill status is provided by reading interrupt request bits IRTXFS(1-0) (bits 2 and 1 in register 2CH).

Transmit PMDL FIFO service interrupts (IRTHIS bit in bit 0 of register 2CH) may be programmed to occur when the transmit PMDL FIFO transitions from more than half full to half empty and/or when the last byte is sent, by setting control bit THIE (bit 1) in register 3DH.

How an End User Might Transmit a PMDL Message

To transmit a PMDL message (79 bytes, excluding flags and FCS-16), first configure the transmitter to generate an interrupt at the end of message by writing a 0 to control bit THIE (bit 1) in register 3DH. Then write a 1 to control bit EHT (bit 0) in register 3DH to enable the transmitter. The transmit PMDL controller will continue to transmit flags until data is written into the transmit PMDL FIFO. Flags are sent in the selected C-bits in the C-bit Parity format DS3 frame as a continuous idle pattern while the transmit PMDL controller is enabled and the transmit PMDL FIFO is empty. If the transmit PMDL controller were not enabled then the PMDL C-bits would be derived from either the external C-bit interface or the internal stuffing logic as dictated by the M13MODE bit (bit 0 in register 02H).

The desired message must be written by the microprocessor into the transmit PMDL FIFO by writing each byte in turn into the TX PMDL FIFO register in register 37H. Bit 0 represents the first bit in the byte to be transmitted.

The bytes written into the TX PMDL FIFO register are transferred automatically into the transmit PMDL FIFO by the M13X. After the microprocessor writes the last byte into the transmit PMDL FIFO, the microprocessor sets the EOM (bit 2) in register 3DH to a 1. The transmit PMDL controller starts processing the message as the PMDL FIFO is written, and continues processing until the FIFO is empty. If it encounters no EOM before the PMDL FIFO becomes empty, the message is aborted. Since the EOM bit was set by the microprocessor, the completion of the message will generate an interrupt, if not masked, as indicated by the interrupt request bit IRTHIS (bit 0) in register 2CH. This latched status indication indicates that the message is complete and another message can be written into the transmit PMDL FIFO by the microprocessor. After the FCS-16 is transmitted (and stuffed by the transmit PMDL controller if needed), the HDLC link controller will start to send flags again.

It is possible to send proprietary messages longer than 79 bytes (excluding FCS plus opening/closing flags). In this case, the THIE bit should be set to a 1. Whenever the transmit PMDL FIFO transitions from more than half full to half empty, then the IRTHIS bit will signal an interrupt request to tell the external microprocessor that there is room to write more data into the transmit PMDL FIFO. This process continues until all of the message has been loaded. Just as in the case above, when the last byte of the message is written by the microprocessor, the EOM bit is set by the microprocessor to identify the end of message to the internal logic so that the FCS can be appended to it.

How an End User Might Receive a PMDL Message

To receive a PMDL message, first configure the receiver to generate an interrupt at the end of message and at the full or overflow level of the receive PMDL FIFO by writing a 0 to control bit RHIE (bit 5) in register 3DH and writing mask bits MIRRHIS(2-0) (bits 7 - 5 in register 35H) to 110 and MIRRXFS(1-0) (bits 4 and 3 in register 35H) to 11. Initialize the receive FIFO by reading the RX PMDL FIFO register in register 38H repeatedly until the receive PMDL FIFO is emptied, which is indicated by RX PMDL FIFO DEPTH = 00H in register 3AH. Then enable the receiver by writing a 1 to control bit EHR (bit 4) in register 3DH.

The receiver will generate an interrupt when the receive PMDL FIFO overflows, is full, or a message has been received. A normal, valid received message is indicated by IRRHIS(2-0) = 010 and IRRXFS(1-0) = 00 or 01. The end user must verify that this is the case. The RX PMDL MESSAGE LENGTH register is then read which gives the end user the number of bytes in the message. The end user then reads that number of bytes from the RX PMDL FIFO register by initiating multiple read cycles. The RX PMDL MESSAGE LENGTH register should be read no more than 212 μs after the IRRHIS(2-0) bits indicate that a message has been received to ensure that a short message does not cause the RX PMDL MESSAGE LENGTH register to be overwritten before the end user could read it.

Please note that the RX PMDL MESSAGE LENGTH register is updated when the end of message event indication is latched and an interrupt is generated, and will not be modified until it is read and cleared by the microprocessor or if another completed message is received. The receive PMDL FIFO must be read for any type of message termination (good FCS, bad FCS, abort, or invalid frame). If an abort occurs the remainder of the HDLC message is discarded, requiring the end user to clear the receive FIFO of the portion of the message indicated by the value in the RX PMDL MESSAGE LENGTH register. Care needs to be taken to determine the location of an aborted message in the receive PMDL FIFO. This can ascertained by reading both the RX PMDL MESSAGE LENGTH and RX PMDL FIFO DEPTH registers. An example is provided to show how to interpret those two registers: An aborted frame is received and an interrupt is signaled via the IRRHIS(2-0) bits. The RX PMDL FIFO DEPTH register is read and found to contain 0AH. The RX PMDL MESSAGE LENGTH register content is read and found to be 07H. This means that there are 3 bytes from a previous frame that need to be read out of the receive PMDL FIFO before the current 7-byte aborted frame can be read out.

Several short messages (such as might occur if several aborted messages are received in succession, or for proprietary messaging) may be left in the receive FIFO and read out at a later time. This is accomplished by storing the message length value read from the RX PMDL MESSAGE LENGTH register and the interrupt requests read from IRLRHIS(2-0) and IRLRXFS(1-0) in a queue. The message boundaries and the validity of the messages read from the FIFO may be determined from interrupt request and message length values. This

practice is not recommended since it complicates the process, requires additional resources and takes extra effort to ensure that the receive PMDL FIFO does not overflow.

If the end user desires to receive a message longer than what could be stored in the receive FIFO, the following procedure can be used: First configure the receiver to generate an interrupt at the end of message or if the receive PMDL FIFO becomes full or overflows by writing a 0 to control bit RHIE (bit 5) in register 3DH and writing mask bits MIRRHIS(2-0) (bits 7 - 5 in register 35H) to 110 and MIRRXFS1,0 (bits 4 and 3) in register 35H to 11. Initialize the receive FIFO by reading the RX PMDL FIFO register in register 38H repeatedly until the FIFO is emptied, which is indicated by RX PMDL FIFO DEPTH = 00H in register 3AH. Then enable the receiver by writing a 1 to control bit EHR (bit 4) in register 3DH.

The receiver will generate an interrupt when the receive PMDL FIFO is full or has overflowed or a message has been received. The end of a normal, valid received message is indicated by IRRHIS(2-0) equal to 010 and IRRXFS(1-0) not equal to 10 or 11. When an interrupt occurs, the end user will read the RX PMDL FIFO DEPTH register and then the IRRXFS(1-0) and the IRRHIS(2-0) bits. If the IRRHIS(2-0) and IRRXFS(1-0) bits indicate that the end of the message has occurred and receive PMDL FIFO full or overflow has not occurred, then the number of bytes indicated by the RX PMDL FIFO DEPTH register is read out of the receive PMDL FIFO since a complete message has been received. If the IRRHIS(2-0) bits do not indicate the end of a message, the IRRHIS(2-0) bits are checked to see the status of the receive PMDL FIFO. If the receive PMDL FIFO is half full, then the end user reads out the message segment indicated by the RX PMDL FIFO DEPTH register and stores it. This process is repeated until the IRRHIS(2-0) bits indicate that the end of a message has been received. If an interrupt occurs while reading a message segment from the receive PMDL FIFO, the process above should be repeated.

In the event that the receive PMDL FIFO overflows, the receive PMDL data will be lost. The receive PMDL FIFO must be cleared out. An FCS error will not necessarily result due to the loss of the data. This is because the FCS is checked before the PMDL data is written into the receive PMDL FIFO. In this case, when the IRRXFS(1-0) bits indicate that the receive PMDL FIFO has overflowed, the RX PMDL FIFO DEPTH register, and perhaps previous values of the RX PMDL MESSAGE LENGTH register (if the receive PMDL FIFO was not empty before the current frame was written to the receive PMDL FIFO) should be used to calculate how much of the data in the receive PMDL FIFO belongs to the corrupted frame. This will allow the end user's software to manage the data in the receive PMDL FIFO and know which data belongs to a good frame and which belongs to a corrupted frame.

COUNTERS

There are up to eight 8-bit or 16-bit performance counters available in the M13X device depending on the setting of the $\overline{M13X}$ lead. The table below describes counter availability. The address shown in the table is that of the low byte for 16-bit counters.

All counters clear when read. All 8-bit counters saturate at a count of FFH. All 16-bit counters saturate at a count of FFFFH and have an associated interrupt request bit to indicate when the counter has saturated. Two read cycles are needed to read a 16-bit counter. A Common Register is provided at address 3EH for storing the high (most significant) byte of a 16-bit counter when its low byte is read. That is, when the low (least significant) byte of a 16-bit counter is read, the high byte of that counter is simultaneously written to the Common Register and can subsequently be read from that register provided that another 16-bit counter read is not performed first. The high byte of a 16-bit counter is not directly accessible via the microprocessor interface; address 3EH must be used to read its contents.

Counter Name	Address (Hex)	$\overline{\text{M13X}}$ lead	Counter Size (Bits)
FEBE Performance Counter (C-bit Parity Mode)/DS3 F-bit and M-bit Error Counter (M13 Mode)	04	Low	16
C-bit Parity Performance Counter (C-bit Parity Mode)/ Number of RX DS3 Frames Counter (M13 Mode)	05	Low	16
P-bit Parity Performance Counter	06	Low	16
DS3 F-bit and M-bit Error Counter	1B	Low	16
C1 Bit Equal to Zero Counter	22	Low	16
DS3 M-bit Error Counter	23	Low	16
RX FCS Error Counter	3B	Low	16
RX ABORT Counter	3C	Low	16
FEBE Performance Counter (C-bit Parity Mode)/DS3 F-bit and M-bit Error Counter (M13 Mode)	04	High	8
C-bit Parity Performance Counter (C-bit Parity Mode)/ Number of RX DS3 Frames Counter (M13 Mode)	05	High	8
P-bit Parity Performance Counter	06	High	8
DS3 F-bit and M-bit Error Counter	1B	High	8
C1 Bit Equal to Zero Counter (Note 1)	22	High	8
DS3 M-bit Error Counter (Note 1)	23	High	8

Notes:

1. This counter is not available when µP1 and µP0 are both set to high.

C-BIT INTERFACES

Transmit and receive DS3 C-bit interfaces are provided for inserting and extracting a set of the DS3 C-bits while operating in C-bit Parity Format mode.

The transmit C-bit interface is comprised of four leads, CCKT (clock output), CDT (data input), CDCCT (data link indication output), and CFMT (frame output). The following DS3 C-bits are accepted at this interface, C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. A control bit C3CLKI is provided in bit 7 of register 19H which can enable or disable the clock pulse for the C3 (FEAC) C-bit. If it is desired to use the internal Transmit FEAC Word register (1CH) or the Remote Loopback register (07H) to transmit FEAC messages and remote loopback requests, then the C3CLKI bit should be set to a 1 to disable the C3 C-bit from being supplied by the external DS3 C-bit interface. If it is desired that the C3 C-bit be derived from external logic instead of the Transmit FEAC Word register, then the C3CLKI bit should be set to a 0 to enable the C3 bit to be sourced from the transmit C-bit interface. When the transmit PMDL controller is enabled, C13, C14, and C15 are supplied by the transmit PMDL Controller, although CCKT will still contain the three clock pulses for those C-bits. When the transmit PMDL controller is disabled, the transmitted C13, C14, and C15 C-bits are taken from the transmit C-bit interface.

The receive C-bit interface is comprised of four leads, CCKR (clock output), CDR (data output), CDCCR (data link indication output), and CFMR (frame output). The following DS3 C-bits are output at this interface: C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. Unlike the transmit C-bit interface, all of the indicated C-bits are always available.

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TEST ACCESS PORT

Introduction

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output leads, as illustrated in 25. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{\text{TRS}}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a two-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the M13X device's internal logic, as illustrated in 25. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in 18.

Boundary scan support

The maximum frequency the M13X device will support for boundary scan is 10 MHz. The M13X device performs the following boundary scan test instructions:

- EXTEST (00)
- SAMPLE/PRELOAD (01)
- BYPASS (11)
- IDCODE (10)

It should be noted that the Capture - IR State (INSTRUCTION_CAPTURE attribute of BSDL) is "01".

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the M13X device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external M13X input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the M13X device remains fully operational. While in this test mode, M13X input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.
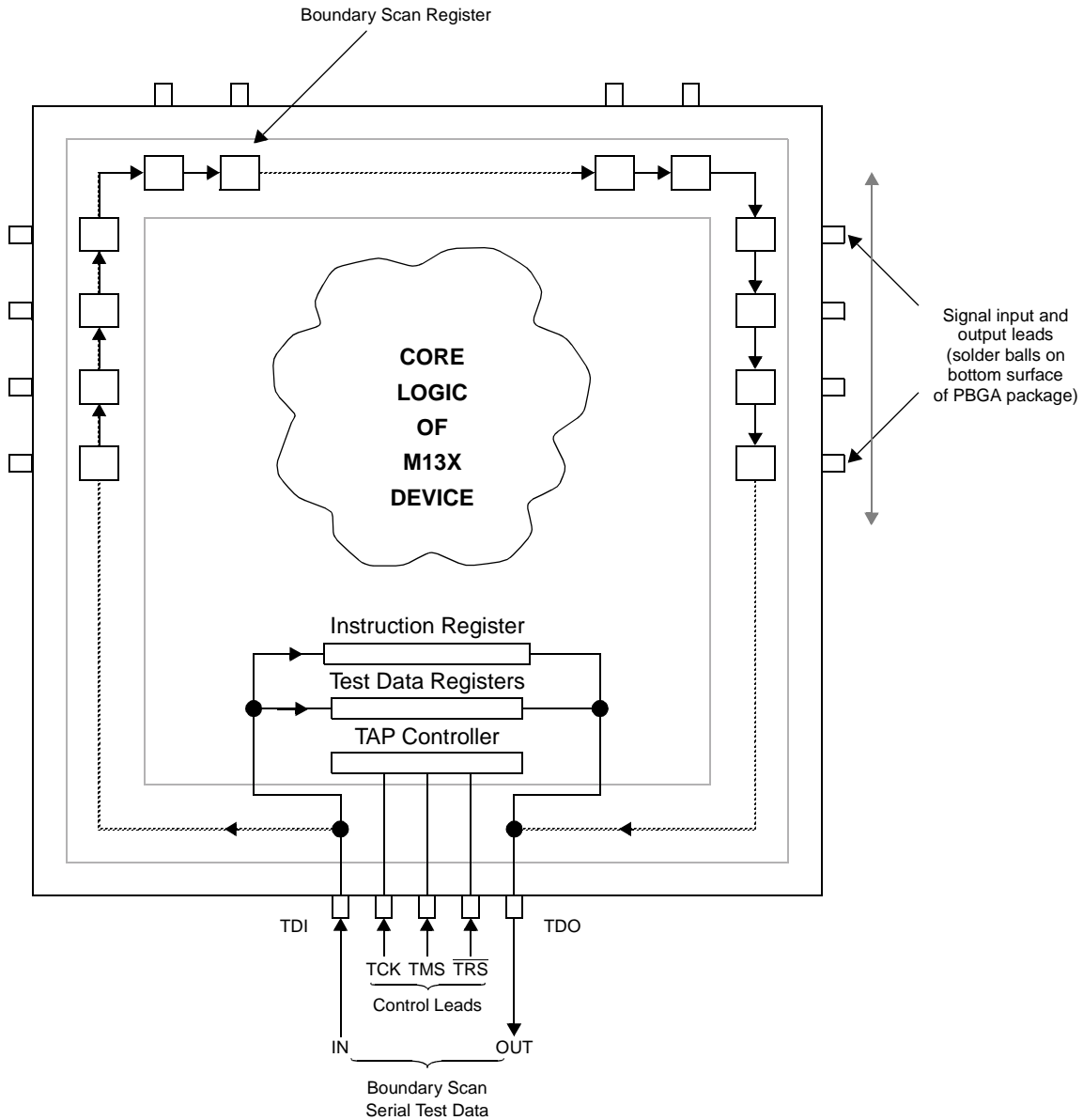
Note: Lead locations are shown for illustration only, and do not correspond to the physical device leads.

Figure 25. Boundary Scan Schematic

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the M13X device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Test Instruction:

When the IDCODE instruction is shifted in, the contents of the IDCODE register can be read. The IDCODE register in the TAP controller consists of the following four fields:

Field	Bit Assignment	Default Value	Comment
M13XREV	31- 28	0000	Revision of the M13X (0 H)
M13XPARTN	27 - 12	0000 1100 1110 1001	M13X Part # (03305 = 0CE9 H)
M13XMANID	11 - 1	000 0110 1011	M13X Manufacturer's ID (TranSwitch = 6B H)
1	0	1	Required bit

Bit 0 is shifted out first.

Boundary scan reset

Specific control of the $\overline{\text{TRS}}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. The lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the TAP controller. If boundary scan testing is to be performed and the lead is held low, then a pull-down resistor value should be chosen which will allow the tester to drive the lead high during test.

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Boundary Scan Chain

There are 177 boundary scan register cells in the boundary scan chain. Scan cell number 0 is defined as the cell nearest the TDO lead and is therefore the first to be shifted out. The last scan cell to be shifted out is number 177. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their function. BSDL files are made available via the Product Software page of the TranSwitch Internet World Wide Web site at www.transwitch.com as they are released.

Scan Cell No.	I/O	Lead No. PQFP	Lead No. PBGA	Symbol	Comments
	I	149	C16	TDI	[SCAN Input]
176	I	161	A15	µP1	Input
175	I	162	B14	µP0	Input
174	--	--	--	--	Tri-State control for cell 173. 1 = Tri-state.
173	O	163	A14	RDY/$\overline{\text{DTACK}}$	Output3
172	--	--	--	--	Internal. Always set to a 0.
171	--	--	--	--	Internal. Always set to a 1.
170	I	165	C13	DT12	Input
169	I	167	D13	CT5	Input
168	I	168	B12	DT5	Input
167	I	169	A12	CT6	Input
166	I	170	C12	DT6	Input
165	I	171	D12	CT7	Input
164	I	172	B11	DT7	Input
163	I	173	A11	CT8	Input
162	I	174	C11	DT8	Input
161	I	175	B10	CT1	Input
160	I	176	A10	DT1	Input
159	I	177	C10	CT2	Input
158	I	178	D10	DT2	Input
157	I	179	A9	CT3	Input
156	I	180	B9	DT3	Input
155	I	181	C9	CT4	Input
154	I	182	D9	DT4	Input
153	--	--	--	--	Tri-State control for CRn and DRn outputs. 1 = Tri-state.
152	O	184	C8	CR19	Output3
151	O	185	A8	DR20	Output3
150	O	186	B8	CR20	Output3

Note: The comments column indicates the functional operation of the corresponding lead.

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Scan Cell No.	I/O	Lead No. PQFP	Lead No. PBGA	Symbol	Comments
149	O	187	D7	DR21	Output3
148	O	188	C7	CR21	Output3
147	O	189	A7	DR22	Output3
146	O	190	B7	CR22	Output3
145	O	192	D6	DR23	Output3
144	O	193	C6	CR23	Output3
143	O	194	A6	DR24	Output3
142	O	195	B6	CR24	Output3
141	O	196	D5	DR25	Output3
140	O	197	C5	CR25	Output3
139	--	--	--	--	Tri-State control for cells 138 and 81. 1 = Tri-state.
138	O	198	A5	CDCCT	Output3
137	O	199	B5	DR26	Output3
136	O	201	A4	CR26	Output3
135	O	202	B4	DR27	Output3
134	O	203	A3	CR27	Output3
133	I	204	B3	DLEN	Input. Cell 139 is used to control CDCCR and CDCCT.
132	I	207	B2	$\overline{\text{HRESET}}$	Input
131	I	3	C3	$\overline{\text{M13X}}$	Input
130	--	--	--	--	Tri-State control for cell 129. 1 = Tri-state.
129	O	4	B1	INT/$\overline{\text{IRQ}}$	Output3
128	O	6	C2	DR28	Output3
127	O	7	D2	CR28	Output3
126	O	8	D3	DR19	Output3
125	O	9	D1	CR18	Output3
124	O	10	D4	DR18	Output3
123	O	11	E2	CR17	Output3
122	O	12	E1	DR17	Output3
121	O	13	E3	CR16	Output3
120	O	14	E4	DR16	Output3
119	O	15	F2	CR15	Output3
118	O	16	F1	DR15	Output3
117	O	17	F3	CR14	Output3

Note: The comments column indicates the functional operation of the corresponding lead.

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Scan Cell No.	I/O	Lead No. PQFP	Lead No. PBGA	Symbol	Comments
116	O	19	G2	DR14	Output3
115	O	20	G1	CR13	Output3
114	O	21	G3	DR13	Output3
113	O	22	G4	CR12	Output3
112	O	23	H2	DR12	Output3
111	O	24	H1	CR11	Output3
110	O	25	H3	DR11	Output3
109	O	26	H4	CR10	Output3
108	O	27	J4	DR10	Output3
107	O	28	J3	CR9	Output3
106	O	29	J1	DR9	Output3
105	O	30	J2	CR8	Output3
104	O	31	K4	DR8	Output3
103	--	--	--	--	Internal. Always set to 1.
102	O	33	L4	CR7	Output3
101	O	34	L3	DR7	Output3
100	O	35	L1	CR6	Output3
99	O	36	L2	DR6	Output3
98	O	37	M4	CR5	Output3
97	O	38	M3	DR5	Output3
96	O	39	M1	CR4	Output3
95	O	40	M2	DR4	Output3
94	O	41	N3	CR3	Output3
93	O	42	N1	DR3	Output3
92	O	43	N2	CR2	Output3
91	O	44	P1	DR2	Output3
90	I	45	P2	A0	Input
89	I	46	R1	A1	Input
88	I	47	T1	A2	Input
87	I	48	R2	A3	Input
86	--	--	--	--	Internal. Always set to 1.
85	I	57	R3	A4	Input
84	I	58	T3	A5	Input
83	I	59	R4	A6	Input
82	I	60	P4	A7	Input

Note: The comments column indicates the functional operation of the corresponding lead.

Scan Cell No.	I/O	Lead No. PQFP	Lead No. PBGA	Symbol	Comments
81	O	61	T4	CDCCR	Output3
80	O	62	N4	CR1	Output3
79	O	63	R5	DR1	Output3
78	O	64	T5	CFMR	Output2
77	O	65	P5	CCKR	Output2
76	O	66	N5	CDR	Output2
75	I	68	T6	DS3CR	Input
74	I	69	P6	DS3DR	Input
73	I	71	P7	$\overline{RD}$,RD/$\overline{WR}$	Input
72	I	72	N7	$\overline{WR}$	Input
71	I	73	R8	ALE	Input
70	I	74	T8	$\overline{SEL}$	Input
69	--	--	--	--	Tri-State control for cells 67, 65, 63, 61, 59, 57, 55, and 53. 1 = Tri-state.
68	I/O	76	N8	A/D7 D7	Input
67	I/O	76	N8	A/D7 D7	Output3
66	I/O	77	N9	A/D6 D6	Input
65	I/O	77	N9	A/D6 D6	Output3
64	I/O	78	P9	A/D5 D5	Input
63	I/O	78	P9	A/D5 D5	Output3
62	I/O	79	T9	A/D4 D4	Input
61	I/O	79	T9	A/D4 D4	Output3
60	I/O	80	R9	A/D3 D3	Input
59	I/O	80	R9	A/D3 D3	Output3
58	I/O	81	N10	A/D2 D2	Input
57	I/O	81	N10	A/D2 D2	Output3
56	I/O	82	P10	A/D1 D1	Input
55	I/O	82	P10	A/D1 D1	Output3
54	I/O	83	T10	A/D0 D0	Input
53	I/O	83	T10	A/D0 D0	Output3
52	--	--	--	--	Internal. Always set to 1.
51	I	85	N11	S7	Input
50	I	86	P11	S6	Input
49	I	87	T11	S5	Input
48	I	89	N12	CDT	Input

Note: The comments column indicates the functional operation of the corresponding lead.

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Scan Cell No.	I/O	Lead No. PQFP	Lead No. PBGA	Symbol	Comments
47	I	90	P12	XCK	Input
46	O	91	T12	CFMT	Output2
45	O	92	R12	CCKT	Output2
44	O	93	P13	DS3DT	Output2
43	I	95	T13	CT25	Input
42	I	96	T14	DT25	Input
41	I	97	R14	CT26	Input
40	I	98	T15	DT26	Input
39	I	99	T16	CT27	Input
38	I	100	R15	DT27	Input
37	--	--	--	--	Internal. Always set to 1.
36	I	108	P14	CT28	Input
35	I	109	R16	DT28	Input
34	I	111	P16	CT21	Input
33	I	112	N15	DT21	Input
32	I	113	N14	CT22	Input
31	I	114	N16	DT22	Input
30	I	115	N13	CT23	Input
29	I	116	M15	DT23	Input
28	I	117	M16	CT24	Input
27	I	118	M14	DT24	Input
26	I	119	M13	CT17	Input
25	I	120	L15	DT17	Input
24	I	121	L16	CT18	Input
23	I	122	L14	DT18	Input
22	I	123	L13	CT19	Input
21	O	125	K16	DS3CT	Output2
20	I	127	K13	DT19	Input
19	I	128	J15	CT20	Input
18	I	129	J16	DT20	Input
17	I	130	J14	CT13	Input
16	I	131	J13	DT13	Input
15	I	132	H13	CT14	Input
14	I	133	H14	DT14	Input
13	I	134	H16	CT15	Input

Note: The comments column indicates the functional operation of the corresponding lead.

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Scan Cell No.	I/O	Lead No. PQFP	Lead No. PBGA	Symbol	Comments
12	I	135	H15	DT15	Input
11	I	136	G13	CT16	Input
10	I	137	G14	DT16	Input
9	I	139	F14	CT9	Input
8	I	140	F16	DT9	Input
7	I	141	F15	CT10	Input
6	I	142	E13	DT10	Input
5	I	143	E14	CT11	Input
4	I	144	E16	$\overline{\text{TXFRM}}$	Input
3	I	145	E15	DT11	Input
2	I	147	D15	CT12	Input
1	--	--	--	--	Internal. Always set to 1.
0	--	--	--	--	Internal. Always set to 1.
	2-State	150	C15	TDO	[SCAN Output]

Note: The comments column indicates the functional operation of the corresponding lead.

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SOFTWARE INITIALIZATION SEQUENCE

The following table lists the sequence that should be followed for initializing the M13X by writing codes to register 1FH:

Register Address	Code (Hex)	Comments
1F (R/W)	F0	Resets internal counters and FIFOs.
1F (R/W)	00	Presets internal counters and FIFOs.

SYSTEM CONSIDERATIONS

Careful attention must be paid to power supply decoupling, device layout, and printed circuit board traces. The M13X has separate +5 volt supply (V_{DD}) leads which provide internal circuit isolation. All V_{DD} leads must be tied together to a single +5 volt power supply in order to avoid excessive substrate currents. TranSwitch recommends that good quality, high frequency, low lead inductance 0.1 microfarad ceramic capacitors be used for decoupling and that they be connected in close proximity to the supply input leads on the device. A decoupling capacitor should be used at each power supply input lead. If low frequency noise is present on the +5 volt supply lead, TranSwitch recommends that a 10 microfarad 6.3 volt tantalum capacitor be connected between +5 volts and ground.

A multilayer board that has separate planes for ground and power should be used. Because of the high data rate at which the M13X operates, it is important that connections between devices be as short as possible. This is especially true for the DS3 receive and transmit interface connections between the M13X and a line interface device, such as the TranSwitch ART, ARTE, DART or DS3LIM-SN. In addition, the clock and data traces should be the same length.

Throughput Delays

The data transmission paths of the M13X device are subject to throughput delays from input to output, as identified in the following table:

Direction	From	To	Delay (min.)	Delay (typ.)	Delay (max.)	Notes
Receive (DJB enabled)	DS3DR	DRn	9920 ns		10520 ns	n = 1 - 28
Receive (DJB disabled)	DS3DR	DRn	200 ns		800 ns	n = 1 - 28
Transmit	DTn	DS3DT	400 ns	4100 ns	7800 ns	n = 1 - 28

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MEMORY MAP

The M13X memory map consists of control bits, alarms (non-latched and latched), and counters that can be accessed via the microprocessor interface. The unused bit positions in a register (shown shaded in the table below) must be masked by software to avoid reading incorrect data. In R/W registers, the shaded positions should be written with a 0. At power-up the memory map will remain random until a hardware reset is initiated via the HRESET lead or a soft reset is applied via register 1FH. This register location is used to reset and initialize the M13X. After power becomes stable, a F0 Hex followed by a 00 Hex must be written into 1FH.

Address (Hex)	Mode (See Note 1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R	R3LOS	R3OOF	R3AIS	R3IDL	R3CKF	T3CKF	XR2	XR1
01	R/W	Test Bit	Test Bit	T3AIS	T3IDL	FEBE	PBITE	CBITE	XT
02	R/W	IDLB	IDLA	Test Bit	3LBK	LPTIME	INVCK	1INV	M13MODE
03	R	CBIT1	DS2OOF7	DS2OOF6	DS2OOF5	DS2OOF4	DS2OOF3	DS2OOF2	DS2OOF1
04	R	FBn: FEBE Performance Counter (C-bit Parity Mode) / DS3 F-bit and M-bit Error Counter (M13 Mode)							
05	R	CPn: C-bit Parity Performance Counter (C-bit Parity Mode) / Number of RX DS3 Frames Counter (M13 Mode)							
06	R	PPn: P-bit parity Performance Counter							
07	R/W	EXEC	CON/DIS	LBSEL	D22	D21	D20	D11	D10
08	R	LBALL	LB25	LB21	LB17	LB13	LB9	LB5	LB1
09	R	LBDS3	LB26	LB22	LB18	LB14	LB10	LB6	LB2
0A	R		LB27	LB23	LB19	LB15	LB11	LB7	LB3
0B	R		LB28	LB24	LB20	LB16	LB12	LB8	LB4
0C	R		LOS25	LOS21	LOS17	LOS13	LOS9	LOS5	LOS1
0D	R		LOS26	LOS22	LOS18	LOS14	LOS10	LOS6	LOS2
0E	R		LOS27	LOS23	LOS19	LOS15	LOS11	LOS7	LOS3
0F	R		LOS28	LOS24	LOS20	LOS16	LOS12	LOS8	LOS4
10	R/W	M13XID0	IDL25	IDL21	IDL17	IDL13	IDL9	IDL5	IDL1
11	R/W		IDL26	IDL22	IDL18	IDL14	IDL10	IDL6	IDL2
12	R/W		IDL27	IDL23	IDL19	IDL15	IDL11	IDL7	IDL3
13	R/W		IDL28	IDL24	IDL20	IDL16	IDL12	IDL8	IDL4
14	R		R2X7	R2X6	R2X5	R2X4	R2X3	R2X2	R2X1
15	R/W		T2X7	T2X6	T2X5	T2X4	T2X3	T2X2	T2X1
16	R(L)	R3LOS	R3OOF	R3AIS	R3IDL	R3CKF	T3CKF	XR2	XR1
17	R(L)	CERROR	DS2OOF7	DS2OOF6	DS2OOF5	DS2OOF4	DS2OOF3	DS2OOF2	DS2OOF1
18		Test Bits							
19	R/W	C3CLKI	Test Bits						
1A	R	RHIS(2-0)			RXFS(1-0)		TXFS(1-0)		
1B	R	FMEn: DS3 F-bit and M-bit Error Counter							
1C	R/W	EXEC	CONT/10	TFEAC6	TFEAC5	TFEAC4	TFEAC3	TFEAC2	TFEAC1
1D	R	FIDL	NEW	RFEAC6	RFEAC5	RFEAC4	RFEAC3	RFEAC2	RFEAC1
1E	R/W	EXEC	CON/DIS		LLB22	LLB21	LLB20	LLB11	LLB10
1F	R/W	RESET and Test Register Mux (See Note 2)							
20	R/W	1TRIST	1LOSSEL	1TAIS1	1TAIS0	1LBV3	1LBV2	1LBV1	1LBV0
21	R/W				R3AIS2	R3AIS1	R3AIS0	T3AIS1	T3AIS0
22	R	C1BZn: C1 Bit Equal to Zero Counter							
23	R	MEn: DS3 M-Bits in Error Counter							

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Address (Hex)	Mode (See Note 1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
24	R(L)	AISXEQ1	AISCEQ0	Test Bits					SEF
25	R(L)	IRLBALL	IRLB25	IRLB21	IRLB17	IRLB13	IRLB9	IRLB5	IRLB1
26	R(L)	IRLBDS3	IRLB26	IRLB22	IRLB18	IRLB14	IRLB10	IRLB6	IRLB2
27	R(L)	IRNEW	IRLB27	IRLB23	IRLB19	IRLB15	IRLB11	IRLB7	IRLB3
28	R(L)	IRSEF	IRLB28	IRLB24	IRLB20	IRLB16	IRLB12	IRLB8	IRLB4
29	R(L)	IRR3LOS	IRR3OOF	IRR3AIS	IRR3IDL	IRR3CKF	IRT3CKF	$\overline{\text{IRXR2}}$	$\overline{\text{IRXR1}}$
2A	R(L)	IRCERROR	IRDS2OOF7	IRDS2OOF6	IRDS2OOF5	IRDS2OOF4	IRDS2OOF3	IRDS2OOF2	IRDS2OOF1
2B	R(L)	IRFCSS	IRABTS	IRFBS	IRCPS	IRPPS	IRFMES	IRC1BZS	IRMES
2C	R(L)	IRRHIS(2-0)			IRRXFS(1-0)		IRTXFS(1-0)		IRTHIS
2D	R(L)								
2E	R/W	MIRLBALL	MIRLB25	MIRLB21	MIRLB17	MIRLB13	MIRLB9	MIRLB5	MIRLB1
2F	R/W	MIRLBDS3	MIRLB26	MIRLB22	MIRLB18	MIRLB14	MIRLB10	MIRLB6	MIRLB2
30	R/W	MIRNEW	MIRLB27	MIRLB23	MIRLB19	MIRLB15	MIRLB11	MIRLB7	MIRLB3
31	R/W	MIRSEF	MIRLB28	MIRLB24	MIRLB20	MIRLB16	MIRLB12	MIRLB8	MIRLB4
32	R/W	MIRR3LOS	MIRR3OOF	MIRR3AIS	MIRR3IDL	MIRR3CKF	MIRT3CKF	MIRXR2	MIRXR1
33	R/W	MIRCERROR	MIRDS2OOF7	MIRDS2OOF6	MIRDS2OOF5	MIRDS2OOF4	MIRDS2OOF3	MIRDS2OOF2	MIRDS2OOF1
34	R/W	MIRFCSS	MIRABTS	MIRFBS	MIRCPS	MIRPPS	MIRFMES	MIRC1BZS	MIRMES
35	R/W	MIRRHIS(2-0)			MIRRXFS(1-0)		MIRTXFS(1-0)		MIRTHIS
36	R/W								
37	W	TX PMDL FIFO (interface register for writing bytes to transmit PMDL FIFO)							
38	R	RX PMDL FIFO (interface register for reading bytes from receive PMDL FIFO)							
39	R	RX PMDL MESSAGE LENGTH							
3A	R	RX PMDL FIFO DEPTH							
3B	R	RX FCS ERROR Counter							
3C	R	RX ABORT Counter							
3D	R/W	DJB	IPOLAL	RHIE	EHR	--	EOM	THIE	EHT
3E	R	CR: Common Register for High Order Counter Byte							
3F	R/W							RISE	FALL

Notes:

1. Read/write (R/W); Read -only (R); Read-only - latched register R(L).

2. F0H followed by 00H resets the entire device.

MEMORY MAP DESCRIPTIONS

Address	Bit	Symbol	Description
00	7	R3LOS	**Receive DS3 Loss of Signal:** A receive DS3 LOS alarm occurs, and this bit is set to 1, when the incoming DS3 data (DS3DR) is stuck low for more than 1020 DS3CR clock cycles. Recovery to 0 occurs when two or more ones are detected in the incoming data bit stream. This bit is intended for board diagnostics and is not meant to indicate a LOS on the DS3 line signal. This bit position is unlatched.
	6	R3OOF	**Receive DS3 Out of Frame:** A receive OOF alarm occurs, and this bit is set to 1, when three out of 16 F-bits are in error utilizing a sliding window of 16 DS3 F-bits, or one or more M-bits are in error in two consecutive frames. Recovery to 0 occurs when the F framing pattern of 1001 is detected, and the M framing pattern of 010 is detected for two consecutive frames. Recovery takes approximately 0.95 milliseconds, worst case. This bit position is unlatched. An OOF also inhibits the performance counters (04H, 05H, 06H, 1BH, 22H, 23H, 3BH, and 3CH).
	5	R3AIS	**Receive AIS Alarm Indication Signal:** The M13X detects DS3 AIS by five methods. The method of detection that drives the R3AIS alarm, and sets this bit to 1, is selected by the states written to the three R3AISn bits in register 21H. This bit position is unlatched. When the M13X is configured to detect one of the framed AIS signals (selected via bits 4-2 of register 21H), the R3OOF bit (bit 6 of this register) should be examined to ensure that the M13X is detecting DS3 frame.
	4	R3IDL	**Receive DS3 Idle Pattern Signal:** A DS3 idle pattern signal has a valid M-frame alignment channel, M-subframe alignment channel, and P-bit channel. The information bits are a 1100 sequence that starts with 11 after each M-frame alignment, M-subframe alignment, X-bit, P-bit, and C-bit channels. The C-bits (C7, C8, and C9) in M-subframe 3 are set to 0. A valid received DS3 idle signal is detected, and this bit is set to 1, when the M13X detects zeros for C7, C8, and C9 in subframe 3 and the 1100 sequence. The M13X searches for the 1100 pattern sequence on a per DS3 frame basis. The M13X can tolerate up to and including 5 errored 4-bit groups of the 1100 pattern per DS3 frame and still recognize the 1100 pattern as valid. If the M13X detects 6 or more errored 4-bit groups of the 1100 pattern per DS3 frame the M13X will exit the R3IDL state and this bit will reset to 0. This bit position is unlatched. A DS3 idle signal as defined in ANSI T1.107-1995 is being received by the M13X device if this bit and bits 1 and 0 of this register are all set to 1.
	3	R3CKF	**Receive DS3 Clock Failure:** A receive DS3 clock failure alarm occurs, and this bit is set to 1, when the receive clock (DS3CR) is stuck high or low for 6-7 XCK clock cycles. Recovery to 0 occurs when the DS3CR clock returns for one cycle. The demultiplexer does not function when the receive clock is lost. The DS3CR lead is still monitored for this alarm during DS3 local loopback (control bit 3LBK = 1), so that it may be necessary to set control bits 1TAIS1 and 1TAIS0 to 11 to prevent AIS insertions into the receive DS1 data stream. This bit position is unlatched.

Address	Bit	Symbol	Description
00 (cont.)	2	T3CKF	**Transmit DS3 Clock Failure:** A transmit DS3 clock failure alarm occurs, and this bit is set to 1, when the transmit input clock (XCK) is stuck high or low for 6-7 DS3CR clock cycles. A failure causes the receive clock to become the transmit clock. This permits the M13X microprocessor interface, multiplexer, and DJB logic to function. Recovery to 0 occurs when the XCK clock returns for one cycle.
	1	XR2	**Receive DS3 X-bit Number 2:** This bit position indicates the receive state of X2. This bit position is updated each frame.
	0	XR1	**Receive DS3 X-bit Number 1:** This bit position indicates the receive state of X1. This bit position is updated each frame.
01	7	Test Bit	**Reserved for TranSwitch Testing Purposes:** A 0 must be written into this bit position.
	6	Test Bit	**Reserved for TranSwitch Testing Purposes:** A 0 must be written into this bit position.
	5	T3AIS	**Transmit DS3 Alarm Indication Signal:** A 1 causes the M13X to transmit a DS3 AIS. The type of AIS sent is determined by the states written into bit 1 (T3AIS1) and bit 0 (T3AIS0) in register 21H.
	4	T3IDL	**Transmit DS3 Idle Signal:** To transmit a DS3 idle signal, (i) a 1 must be written in this bit 4 (T3IDL) register location, and (ii) a 1 must also be written (if not already written) into bit 0 (XT) of this register 01H, and (iii) bit 0 (T3AIS0) and bit 1 (T3AIS1) of register 21H must also be set to 0.
	3	FEBE	**Transmit Far End Block Error:** A 1 causes the M13X to transmit a single FEBE error indication (C10, C11, and C12 equal to 0) in the next DS3 frame. This bit is not self-clearing; to send an additional FEBE indication, the microprocessor must first write this bit with a 0 and then with a 1.
	2	PBITE	**Transmit P-Bit Parity Error:** A 1 causes the M13X to transmit a single P-bit parity error in the next DS3 frame. The P-bit error is transmitted by inverting the value of the two calculated bits. This bit is not self-clearing; to send an additional error, the microprocessor must first write this bit with a 0 and then with a 1.
	1	CBITE	**Transmit C-Bit Parity Error:** A 1 causes the M13X to transmit a single C-bit parity error in the next available DS3 frame when the M13X is operating in the C-bit parity mode. The C-bit error is transmitted by inverting the calculated C-bit parity bits in subframe 3 (C7, C8, and C9). This bit is not self-clearing; to send an additional error, the microprocessor must first write this bit with a 0 and then with a 1.
	0	XT	**Transmit X-Bits:** The X-bits may be used to transmit a yellow alarm or may be used as a low speed signaling channel. A 1 or 0 causes the M13X to transmit a 1 or 0 for both X1 and X2. Note: This bit must be set to 1 when transmitting DS3 idle signal (see T3IDL, bit 4 in this register 01H).

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Address	Bit	Symbol	Description
02	7 6	IDLB IDLA	**DS1 Idle Code Selection:** Three DS1 idle codes are provided, as shown in the table below. The idle code selected via these control bits is common to all DS1 channels selected for idle code transmission. One or more transmitted DS1 channels is selected by writing a 1 in the corresponding IDLn bit(s) in register locations 10H, 11H, 12H, and 13H, provided register location 1EH has not been set so as to select that DS1 channel for loopback. IDLB IDLA DS1 Idle Code Selected 0 0 Quasi-Random Signal (2^{20} - 1 QRS) including zero suppression. 1 0 Framed Extended Super Frame (ESF) signal format which consists of an S-bit pattern of 001011 in every fourth signaling bit position, CRC-6 pattern, and ones in the 64 kbit/s channels 1 through 24. X 1 Unframed all ones signal (AIS).
	5	Test Bit	**Reserved for TranSwitch Testing Purposes:** A 0 must be written into this bit position.
	4	3LBK	**DS3 Local Loopback:** A 1 disables the DS3 receive input and causes the DS3 transmit output to be looped back as receive data. Transmit data is provided at the output (DS3DT). Please note that the DS3CR lead is still monitored for a R3CKF alarm
	3	LPTIME	**Receive Loop Timing:** A 1 disables the external transmit clock input (XCK), and causes the DS3 receive clock to become the DS3 transmit clock. If the DS3 receive clock fails in this mode, the M13X switches over to the transmit clock (XCK). The demultiplexer becomes inoperative, but the multiplexer and microprocessor interface continue to function.
	2	INVCK	**Invert DS1 Transmit Clocks:** A 1 causes all transmit DS1 data inputs (DTn) to be sampled on the falling edges of their respective DS1 clock inputs (CTn). This is provided for back-to-back M13X operation.
	1	1INV	**Invert DS1 Transmit Data:** A 1 causes the transmit data inputs for all DS1 channels (DTn) to be inverted within the M13X.
	0	M13MODE	**M13 Operating Mode:** A 1 enables the M13X to operate in the M13 format mode. Using ANSI T1.107-1995 terminology, the M13X performs M12 mode and M23 mode muxing and demuxing where the DS2 and DS3 C-bits are used for stuffing/destuffing. A 0 enables the M13X to operate in the C-bit parity mode as specified in the ANSI T1.107-1995.
03	7	CBIT1	**C-bit Number 1 State:** This bit is updated each frame with the state of the received C1 bit. The C1 bit is used to identify the DS3 application according to the table shown below: C1 Value Application Random M13 format All 1s C-bit parity format In addition, any C-bit that is received as 0 will increment the C-bit Equal to Zero Counter in register 22H.

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Address	Bit	Symbol	Description
03 (cont.)	6-0	DS2OOFn (n=7-1)	**DS2 Out of Frame Alarm Indication:** A 1 in bits 6-0 corresponds to an Out Of Frame alarm for the corresponding DS2 channel (7-1). A DS2 OOF occurs when two out of four consecutive framing bits are in error. A DS2 OOF for a DS2 channel causes AIS to be inserted into its four DS1 channels when 1TAIS1, 1TAIS0 = 0, 0 or 0, 1 in register 20H, bits 5 and 4. Recovery to 0 is based on searching for the 0101 framing pattern. Framing is accomplished by starting at an arbitrary point with the first received bit (0 or 1) and looking 147 (3x49) bit positions later for the bit of opposite sense. This search is performed for 12 bit positions simultaneously. Once the framing pattern is found, one more frame is used to acquire alignment. Recovery takes approximately 6.8 milliseconds, worst case average.
04	7-0	FBn (n=7-0)	**FEBE Performance Counter/DS3 F-Bit and M-Bit Error Counter:** This performance counter counts the number of FEBEs received since the last read cycle in the C-bit parity mode. A FEBE indication occurs when C10, C11, or C12 is received equal to 0 in a DS3 frame. The counter is protected during the period of a microprocessor read cycle and when the M13X is attempting to write to the counter. When this occurs, the incoming error count indication is held until the counter is read and cleared. Afterwards, the counter increments. Only the indication of one error count is held during the microprocessor read and the M13X write cycle. The counter is also inhibited during DS3 loss of signal or out of frame times. This counter is cleared when it is read by the microprocessor. In the M13 format mode, this saturating counter counts the number of DS3 F-bits and M-bits that have been received in error. This counter is inhibited when a DS3 OOF occurs and clears when read. When lead $\overline{M13X}$ is low, this counter is 16 bits wide and this address contains the low byte of the counter. The high byte of this counter is written to the CR register (3EH) when this register is read. When $\overline{M13X}$ is high, this counter is 8 bits wide.
05	7-0	CPn (n=7-0)	**C-Bit Parity Performance/Number of Frames Counter:** In the C-bit parity mode, this counter counts the number of C-bit parity errors received since the last read cycle. In the M13 format mode, it counts the number of DS3 frames since the last read cycle. The counter is protected during the period of a microprocessor read cycle and when the M13X is attempting to write to the counter. When this occurs, the incoming error count indication is held until the counter is read and cleared. Afterwards, the counter increments. Only the indication of one error count is held during the microprocessor read and the M13X write cycle. The counter is inhibited during DS3 loss of signal or out of frame times, and is cleared when it is read by the microprocessor. When lead $\overline{M13X}$ is low, this counter is 16 bits wide and this address contains the low byte of the counter. The high byte of this counter is written to the CR register (3EH) when this register is read. When $\overline{M13X}$ is high, this counter is 8 bits wide.
06	7-0	PPn (n=7-0)	**P-Bit Parity Performance Counter:** This counter counts the number of P-bit parity errors received since the last read cycle. This performance count is valid in either operating mode. The counter is protected during the period of a microprocessor read cycle and when the M13X is attempting to write to the counter. When this occurs, the incoming error count indication is held until the counter is read and cleared. Afterward, the counter increments. Only the indication of one error count is held during the microprocessor read and the M13X write cycle. The counter is also inhibited during DS3 loss of signal or out of frame times. This counter is cleared when it is read by the microprocessor. When lead $\overline{M13X}$ is low, this counter is 16 bits wide and this address contains the low byte of the counter. The high byte of this counter is written to the CR register (3EH) when this register is read. When $\overline{M13X}$ is high, this counter is 8 bits wide.

Address	Bit	Symbol	Description
07	7 6 5 4 3 2 1 0	EXEC CON/DIS LBSEL D22 D21 D20 D11 D10	**Remote Loopback:** The bits in this location are used to send a DS1 remote loopback request in the M13 format mode, or a DS3/DS1 remote loopback request in the C-bit parity mode (See Note 1). Bit 7 (EXEC) executes the command. Bit 6 (CON/DIS, see Note 2) selects the command to connect or disconnect the loopback selected. When in C-bit parity mode bit 5 (LBSEL) selects either DS2 C or stuff bit inversions, defined by the four 1LBVn bits in register 20H or a double FEAC message (in C-bit parity mode only) when sending a loopback request. The DS2 C or stuff bit inversion mechanism in the M13 (or C-bit parity) format mode is selected by the states written to the four 1LBVn bits in register 20H. Bits 4 (D22), 3 (D21), and 2 (D20) select the DS2 channels (1-7). Bits 1 (D11) and 0 (D10) select one of four DS1 channels. In the C-bit Parity mode, the FEAC channel (C3) can be used for sending DS1 and DS3 remote loopback requests. The channel to be looped is written into bits 4-0. The M13X translates this code into the FEAC codeword. To send a loopback request using the FEAC channel, the M13X sends 10 repetitions of the FEAC line activator code sequence (0 000111 0 11111111) followed immediately by 10 repetitions of the loopback codeword (0 xxxxxx 0 11111111). At the end of this sequence (20 codewords or 320 DS3 frames), completion is indicated by bit 7 (EXEC) resetting to 0. To deactivate a loopback using the FEAC channel, the M13X sends 10 repetitions of the deactivate code followed immediately by 10 repetitions of the channel selected. The codes for sending and deactivating a remote loopback request are shown below:

Bits Channel	7 EXEC	6 CON/DIS	5 LBSEL	4 D22	3 D21	2 D20	1 D11	0 D10
All	1	1 or 0	X	0	0	0	0	0
Channel 1	1	1 or 0	X	0	0	1	0	0
Channel 2	1	1 or 0	X	0	0	1	0	1
Channel 28	1	1 or 0	X	1	1	1	1	1
DS3	1	1 or 0	1	0	0	0	1	0

Notes:
For CON/DIS, Connect = 1, Disconnect = 0
For X, 1 = FEAC (C-bit parity mode only), 0 = DS2 C or stuff bit inversion

Notes:
1. If this register is used to send a remote loopback request using the double word FEAC message then the C3CLKI bit in register 19 Hex must be set to a 1.
2. CON/DIS is not used when LBSEL = 0. Instead, bit 7 (EXEC) is used when LBSEL = 0 to send (EXEC = 1) or stop sending (EXEC = 0) a remote loopback request via the DS2 C or stuff bit inversions defined by register 20H bits 3-0. If a loopback request for a different channel is sent via register 07H (that uses DS2 C or stuff bit inversion), the current transmitted loopback request is taken down. i.e. only single loopback requests can be sent one at a time unless the "all" loopback request command is used. When the "all" loopback request command is used, loopback requests for all channels are simultaneously transmitted.

Address	Bit	Symbol	Description
08	7 6 5 4 3 2 1 0	LBALL LB25 LB21 LB17 LB13 LB9 LB5 LB1	**Receive Loopback Requests:** Bit 7, LBALL (all DS1 channels), bits 6-0 (LBn), and registers 09H through 0BH indicate the loopback request detected. For the M13 format mode, a loopback request is received when any of the conditions (DS2 C-bit or stuff) are detected five or more times in succession. The remote loopback selection is determined by the states written to the 1LBVn bits in register location 20H. A remote loopback request is cancelled when the normal state of the bit is received five or more times in succession. In the C-bit parity mode, a remote loopback request is received by detecting the FEAC connect word five times in succession, followed by five consecutive receptions of the DS1 channel number word. A remote loopback request is cleared upon the reception of five consecutive disconnect FEAC messages followed by the reception of the DS1 channel number word. The M13X will also respond to the conditions (DS2 C-bit or stuff) set up by the 1LBVn bits in register location 20H while in C-bit parity mode. Note: It is possible to have multiple loopbacks set. Once a loopback request is received or taken down in registers 08H-0BH, the microprocessor must write the appropriate code to register 1EH to correspondingly set up or take down the loopback in the appropriate DS1 channel. When detecting loopback requests via the mechanism indicated by the 1LBVn bits in register 20H, the M13X must have DS2 and DS3 frame synchronization. When detecting loopback requests via the FEAC channel, the M13X must have DS3 frame synchronization and not be receiving DS3 AIS or DS3 Idle signals. LBALL is valid only in C-bit parity mode.
09	7 6 5 4 3 2 1 0	LBDS3 LB26 LB22 LB18 LB14 LB10 LB6 LB2	**Receive Loopback Requests:** Bits 7 (LBDS3), 6-0 (LBn), and registers 08H, 0AH and 0BH indicate loopback requests sent by the distant end for either a DS3 loopback or for the DS1 channels indicated. For complete explanation, see 08H. LBDS3 is valid only in C-bit parity mode.
0A	7	Reserved	**Reserved:** This bit should always be ignored.
	6 5 4 3 2 1 0	LB27 LB23 LB19 LB15 LB11 LB7 LB3	**Receive Loopback Requests:** Bits 6-0 (LBn) and registers 08H, 09H and 0BH indicate loopback requests sent by the distant end for the DS1 channels indicated. For complete explanation, see 08H.
0B	7	Reserved	**Reserved:** This bit should always be ignored.
	6 5 4 3 2 1 0	LB28 LB24 LB20 LB16 LB12 LB8 LB4	**Receive Loopback Requests:** Bits 6-0 (LBn) and registers 08H through 0AH indicate loopback requests sent by the distant end for the DS1 channels indicated. For complete explanation, see 08H.

Address	Bit	Symbol	Description
0C	7	Reserved	**Reserved:** This bit should always be ignored.
	6 5 4 3 2 1 0	LOS25 LOS21 LOS17 LOS13 LOS9 LOS5 LOS1	**Loss of Signal, DS1 Channel n:** Each DS1 channel is monitored for loss of signal, which sets the associated bit LOSn to 1. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state written to control bit 1LOSSEL, bit 6 in register 20H. A 1 selects the transmit DS1 channels. A DS1 channel loss of signal is defined as between eight and sixteen DS2 frames of consecutive 0s. Recovery occurs after the first 1 is detected.
0D	7	Reserved	**Reserved:** This bit should always be ignored.
	6 5 4 3 2 1 0	LOS26 LOS22 LOS18 LOS14 LOS10 LOS6 LOS2	**Loss of Signal, DS1 Channel n:** Each DS1 channel is monitored for loss of signal, which sets the associated bit LOSn to 1. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state written to control bit 1LOSSEL, bit 6 in register 20H. A 1 selects the transmit DS1 channels. A DS1 channel loss of signal is defined as between eight and sixteen DS2 frames of consecutive 0s. Recovery occurs after the first 1 is detected.
0E	7	Reserved	**Reserved:** This bit should always be ignored.
	6 5 4 3 2 1 0	LOS27 LOS23 LOS19 LOS15 LOS11 LOS7 LOS3	**Loss of Signal, DS1 Channel n:** Each DS1 channel is monitored for loss of signal, which sets the associated bit LOSn to 1. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state written to control bit 1LOSSEL, bit 6 in register 20H. A 1 selects the transmit DS1 channels. A DS1 channel loss of signal is defined as between eight and sixteen DS2 frames of consecutive 0s. Recovery occurs after the first 1 is detected.
0F	7	Reserved	**Reserved:** This bit should always be ignored.
	6 5 4 3 2 1 0	LOS28 LOS24 LOS20 LOS16 LOS12 LOS8 LOS4	**Loss of Signal, DS1 Channel n:** Each DS1 channel is monitored for loss of signal, which sets the associated bit LOSn to 1. The selection of monitoring transmit DS1 channels or receive DS1 channels is determined by the state written to control bit 1LOSSEL, bit 6 in register 20H. A 1 selects the transmit DS1 channels. A DS1 channel loss of signal is defined as between eight and sixteen DS2 frames of consecutive 0s. Recovery occurs after the first 1 is detected.
10	7	M13XID0	**Device ID 0:** This bit is used to identify whether an M13X or an M13E device is installed in an application. If this bit is always 0 then the device is an M13X device. If this bit is a read/write bit then it is an M13E device. The M13E device is the predecessor of the M13X device.
	6 5 4 3 2 1 0	IDL25 IDL21 IDL17 IDL13 IDL9 IDL5 IDL1	**Internal DS1 Idle Channel/Loopback:** The IDLn bits in this register are used for generating and transmitting a DS1 idle pattern or for setting up a local DS1 loopback for channel n. When register 1EH is written with a code to disconnect the loopback on a channel in this register, and the corresponding IDLn bit is written with a 1, the M13X generates and transmits a DS1 idle pattern in that channel which is determined by the idle code selection bits (IDLB and IDLA in location 02H). When a code to connect a loopback on a channel in this register is written to register 1EH, and a 1 is written into the corresponding IDLn bit, the DS1 channel is looped back instead. The loopback is from the receive to the transmit direction. When the IDLn bit is written with a 0, the DS1 transmit source is from the channel's DTn/CTn leads.

Address	Bit	Symbol	Description
11	7	Reserved	**Reserved:** This bit should always be written with a 0.
	6 5 4 3 2 1 0	IDL26 IDL22 IDL18 IDL14 IDL10 IDL6 IDL2	**Internal DS1 Idle Channel/Loopback:** The IDLn bits in this register are used for generating and transmitting a DS1 idle pattern or for setting up a local DS1 loopback for channel n. When register 1EH is written with a code to disconnect the loopback on a channel in this register, and the corresponding IDLn bit is written with a 1, the M13X generates and transmits a DS1 idle pattern in that channel which is determined by the idle code selection bits (IDLB and IDLA in location 02H). When a code to connect a loopback on a channel in this register is written to register 1EH, and a 1 is written into the corresponding IDLn bit, the DS1 channel is looped back instead. The loopback is from the receive to the transmit direction. When the IDLn bit is written with a 0, the DS1 transmit source is from the channel's DTn/CTn leads.
12	7	Reserved	**Reserved:** This bit should always be written with a 0.
	6 5 4 3 2 1 0	IDL27 IDL23 IDL19 IDL15 IDL11 IDL7 IDL3	**Internal DS1 Idle Channel/Loopback:** The IDLn bits in this register are used for generating and transmitting a DS1 idle pattern or for setting up a local DS1 loopback for channel n. When register 1EH is written with a code to disconnect the loopback on a channel in this register, and the corresponding IDLn bit is written with a 1, the M13X generates and transmits a DS1 idle pattern in that channel which is determined by the idle code selection bits (IDLB and IDLA in location 02H). When a code to connect a loopback on a channel in this register is written to register 1EH, and a 1 is written into the corresponding IDLn bit, the DS1 channel is looped back instead. The loopback is from the receive to the transmit direction. When the IDLn bit is written with a 0, the DS1 transmit source is from the channel's DTn/CTn leads.
13	7	Reserved	**Reserved:** This bit should always be written with a 0.
	6 5 4 3 2 1 0	IDL28 IDL24 IDL20 IDL16 IDL12 IDL8 IDL4	**Internal DS1 Idle Channel/Loopback:** The IDLn bits in this register are used for generating and transmitting a DS1 idle pattern or for setting up a local DS1 loopback for channel n. When register 1EH is written with a code to disconnect the loopback on a channel in this register, and the corresponding IDLn bit is written with a 1, the M13X generates and transmits a DS1 idle pattern in that channel which is determined by the idle code selection bits (IDLB and IDLA in location 02H). When a code to connect a loopback on a channel in this register is written to register 1EH, and a 1 is written into the corresponding IDLn bit, the DS1 channel is looped back instead. The loopback is from the receive to the transmit direction. When the IDLn bit is written with a 0, the DS1 transmit source is from the channel's DTn/CTn leads.
14	7	Reserved	**Reserved:** This bit should always be ignored.
	6-0	R2Xn (n=7-1)	**Receive DS2 X-Bits:** The bits in this location indicate the states of the seven received DS2 channel X-bits.
15	7	Reserved	**Reserved:** This bit should always be written with a 0.
	6-0	T2Xn (n=7-1)	**Transmit DS2 X-bits:** The bits in this location are used to set the states of the seven transmitted DS2 channel X-bits. An X-bit off state is normally a 1.
16	7 6 5 4 3 2 1 0	R3LOS R3OOF R3AIS R3IDL R3CKF T3CKF $\overline{XR2}$ $\overline{XR1}$	**Latched Receive Alarms/Status:** The bits in this register location are the same alarm/status bits listed in register location 00H, except the corresponding bit latches on with an alarm. Bits 1 and 0 are the latched inverses of the two X-bits received. When latched on they are equal to 0. A microprocessor read cycle clears all these bits to their off states. If an alarm state or status condition remains true, the corresponding bit relatches.

Address	Bit	Symbol	Description
17	7 6-0	CERROR DS2OOFn (n=7-1)	**Latched C-bit Status/DS2 Out Of Frame Bits:** The bits in this register are the same bits listed in register location 03H, except the corresponding bit latches on with an alarm. For example, CERROR latches to a 1 the first time C1 is 0. A microprocessor read cycle clears all latched bits. If a DS2 OOF remains true, the corresponding bit relatches.
18	7-0	Test Bits	**TranSwitch Test Register:** Used for TranSwitch testing. This register must not be written.
19	7	C3CLKI	**C-Bit Parity C3 Clock Inhibit:** A 0 enables the M13X to generate an extra clock pulse in the CCKT clock signal for clocking the C3 bit in from external logic. A 1 disables the generation of the C3 clock pulse. This bit must be set to 1 if the FEAC register 1CH is used to transmit FEAC codes or if register 07H is used to send a remote loopback request via a double word FEAC message (LBSEL = 1). If this bit is set to 0, then the FEAC messages are derived from the external C-bit interface.
	6-0	Test Bits	**TranSwitch Test Bits:** Used for TranSwitch testing. When this register is written, the values read from these bits must be re-written.
1A	7-5	RHIS2- RHIS0	**Receive PMDL Status:** The following table lists the various status indications associated with the receive PMDL message. The significance of these bits is controlled by control bit RHIE (bit 5) in register 3DH.

RHIS2	RHIS1	RHIS0	RHIE	Condition Present
0	0	0	X	Idle condition
0	0	1	X	Start of message indication
0	1	0	0	Valid message received; (FCS checked OK), or the receive FIFO needs servicing (full or overflow).
0	1	0	1	Valid message received; (FCS checked OK), or the receive FIFO needs servicing (half full or more).
0	1	1	X	Message received with FCS error
1	0	0	X	Abort message received
1	1	1	X	Invalid Frame received. (i.e., a frame with a non-integral number of bytes or with a number of bytes (after destuffing) less than 5).
1	0	1	X	Unused Code. See note below.
1	1	0	X	Unused code. (Make sure that bit-oriented codes, do not cause these bits to become set). This combination of bit settings should never appear.

These are unlatched bits that reflect the current status of the receive PMDL processing. Codes of 101 and 110 are not defined. When a condition occurs, all three bits are updated at once and are typically set for at least 1 byte time (i.e., 8 receive PMDL bits) after which they are reset to 0.

The priority for detecting these alarms is:

- Abort (highest)
- Invalid Frame Received
- FCS Error Received
- Start of Message Indication
- Valid Message Received

Address	Bit	Symbol	Description
1A (cont.)	4-3	RXFS1-RXFS0	**Receive PMDL FIFO Status:** The following table lists the various FIFO status indications associated with the receive PMDL FIFO. <table><tr><td>RXFS1</td><td>RXFS0</td><td>Condition Present</td></tr><tr><td>0</td><td>0</td><td>Normal. PMDL FIFO less than half full.</td></tr><tr><td>0</td><td>1</td><td>FIFO equal to or more than half full</td></tr><tr><td>1</td><td>0</td><td>FIFO full</td></tr><tr><td>1</td><td>1</td><td>FIFO overflow</td></tr></table> These are unlatched bits that indicate the current state of the receive PMDL FIFO. When a condition occurs both bits are updated at once.
	2-1	TXFS1-TXFS0	**Transmit PMDL FIFO Status:** The following table lists the various FIFO status indications associated with the transmit PMDL FIFO. <table><tr><td>TXFS1</td><td>TXFS0</td><td>Condition Present</td></tr><tr><td>0</td><td>0</td><td>Normal. PMDL FIFO equal to or more than half full</td></tr><tr><td>0</td><td>1</td><td>FIFO less than half full</td></tr><tr><td>1</td><td>0</td><td>FIFO overflowed (attempt to write to a full FIFO)</td></tr><tr><td>1</td><td>1</td><td>FIFO underflow. Reported only if EOM not set when FIFO underflows.</td></tr></table> These are unlatched bits that indicate the current state of the transmit PMDL FIFO. When a condition occurs both bits are updated at once.
	0	Reserved	**Reserved:** This bit is reserved and the value read from it must be ignored.
1B	7-0	FMEn (n=7-0)	**DS3 F-Bits and M-Bits in Error Counter:** A saturating counter that counts the number of DS3 F-bits and DS3 M-bits that are in error since it was last read. The counter is inhibited when DS3 loss of signal or out of frame occurs. The counter is cleared when it is read by the microprocessor. When $\overline{\text{M13X}}$ is low, this counter is 16 bits wide and this address contains the low byte of the counter. The high byte of this counter is written to the CR register (3EH) when this register is read. When $\overline{\text{M13X}}$ is high, this counter is 8 bits wide.

Address	Bit	Symbol	Description
1C	7 6 5-0	EXEC CONT/10 TFEACn (n=6-1)	**Transmit FEAC Word:** Bit 7 (EXEC) initiates the FEAC transmission and also indicates when the transmission is completed. Bit 6 (CONT/10) controls the duration of the FEAC transmission (1 = continuous, 0 = 10 times). Bits 5-0 (TFEACn) constitute the 6-bit variable (XXXXXX) field in the FEAC word. A FEAC word is written in the field in the same order of transmission as shown below: **16-Bit FEAC Word** FEAC Word/ Register 1CH Relationship The M13X formats and generates the other 1s and zeros that comprise the FEAC word. A minimum length (send FEAC word 10 times) message is sent by using the following sequence: • Write 1 0 X X X X X X (XXXXXX = 6-bit FEAC word) • M13X sends 16-bit FEAC word 10 times • M13X indicates completion by resetting bit 7 (0 0 X X X X X X) A continuous FEAC word is sent by using the following sequence: • Write 1 1 X X X X X X (XXXXXX= 6-bit FEAC word) • M13X sends 16-bit FEAC word continuously • Write 1 0 Y Y Y Y Y Y (Y = Don't Care) • M13X terminates FEAC word transmission. Termination is completed when the EXEC bit is set to 0 by the M13X. • Transmission must be terminated before another FEAC word can be loaded and transmitted. Note: The C3CLKI bit in register 19H must be set to a 1 if this register is used to transmit a FEAC message.

Address	Bit	Symbol	Description
1D	7 6 5-0	FIDL NEW RFEACn (n=6-1)	**Receive Single FEAC Word:** Bit 7 (FIDL) is the FEAC idle channel indication. It clears whenever a 0 C3 bit is received framing the six-bit variable word. Bit 7 cannot be reset by a microprocessor read cycle. Bit 6 (NEW) indicates when a new FEAC word has been detected. It clears when the register is read. When the $\overline{\text{M13X}}$ lead is high, the NEW bit will be set under the conditions that cause the NEW bit to be set in the M13E device. Namely, the NEW bit becomes set when any five consecutive and identical FEAC messages are received. The NEW bit will continually be reasserted if it is read and cleared when a continuous constant FEAC message is received. When the $\overline{\text{M13X}}$ lead is low, the NEW bit does not become set to one again after it is cleared when a continuous constant FEAC message is received. Bits 5-0 (RFEACn) constitute the variable (XXXXXX) field in the FEAC word. A received FEAC word is stored in bits 5-0 with the first bit received in bit 0, as shown below: **16-Bit FEAC Word** `0  X X X X X X  0  1 1 1 1 1 1 1 1` Bit 7 `        X X X X X` 1DH The following table lists possible FEAC combinations: FIDL NEW Status 1 0 FEAC channel idle - No message received since last read cycle 0 1 New message received - FEAC channel busy 1 1 New message received - FEAC channel idle Notes: 1. There is no buffering for the received FEAC message. The latest, validated FEAC message is stored and bit 6 (NEW) is set to 1 even if the previous message was not read. 2. Line loopback activate and deactivate FEAC codes are not displayed in this register. Also the individual line loopback activate and deactivate codewords are not displayed in this register.

Address	Bit	Symbol	Description
1E	7 6 5 4 3 2 1 0	EXEC CON/DIS Reserved LLB22 LLB21 LLB20 LLB11 LLB10	**DS1 Local Loopback:** This register is used in conjunction with registers 10H-13H. Bit 7 (EXEC) initiates the loopback. This bit is reset automatically upon completion of the command. Bit 6 (CON/DIS) connects or disconnects the specified loopback. Bit 5 is reserved and must be written with a 0. Bits 4 through 2 (LLB2n) select one of seven DS2s. Bits 1 and 0 (LLB1n) select the DS1 within the DS2 signal. The following table lists the commands for generating local loopback:
1F	7-0	RESET	**Initialization Register:** This register location is used to reset and initialize the M13X. After power becomes stable, a F0 Hex followed by a 00 Hex must be written into this location.

Bits Channel	7 EXEC	6 CON/ DIS	5 Res.	4 LLB22	3 LLB21	2 LLB20	1 LLB11	0 LLB10
All	1	1	0	0	0	0	0	0
Clear All	1	0	0	0	0	0	0	0
Clear All Confirmed	0	0	0	0	0	0	0	0
Channel 1	1	1	0	0	0	1	0	0
Channel 2	1	1	0	0	0	1	0	1
Channels 3 to 27	11000110 to 11011110, LLB2 incrementing on LLB1=00							
Channel 28	1	1	0	1	1	1	1	1
Clear Channel 28	1	0	0	1	1	1	1	1
Clear Channel 28 Confirmed	0	0	0	1	1	1	1	1

Address	Bit	Symbol	Description
20	7	1TRIST	**Tri-State DS1 Receive Channels:** A 1 causes all 28 receive DS1 data (DRn) and clock (CRn) output leads to be set to a high impedance state.
	6	1LOSSEL	**DS1 Loss of Signal Selection:** A 0 selects the receive DS1 channels for loss of signal detection. A 1 selects the transmit DS1 channels for loss of signal detection. The DS1 loss of signals (LOSn) are reported in register locations 0CH through 0FH.
	5 4	1TAIS1 1TAIS0	**DS1 AIS Insertion Selection:** These two bits control the insertion of AIS (unframed all 1s) into the 28 DS1 channels on certain DS3 alarm conditions that are defined in register location 00H. The following table lists the settings for having various alarm conditions selected to cause AIS: 1TAIS1　1TAIS0　Received DS3 Alarm Conditions 　0　　　　0　　　R3OOF, R3AIS, R3LOS, R3CKF 　0　　　　1　　　R3OOF, R3AIS, R3CKF 　1　　　　0　　　R3LOS 　1　　　　1　　　No AIS insertions For the settings of 1TAIS1 and 1TAIS0 other than 0,0, the DS1 clock and data outputs of the M13X go to one level for those cases where a received DS3 alarm condition that is not supposed to produce a receive DS1 AIS condition occurs. The XCK clock is used as the timebase for generating the DS1 AIS clocks.
	3 2 1 0	1LBV3 1LBV2 1LBV1 1LBV0	**Remote Loopback Options:** The following table indicates the various ways the M13X can transmit and receive a DS1 remote loopback request in the M13 or C-bit parity operating modes. The specified condition is transmitted for the duration of the loopback request (see register 07H for transmission operation): 1LBV3　1LBV2　1LBV1　1LBV0　Loopback Type 　0　　　0　　　0　　　0　　Third DS2 C-bit inverted 　0　　　0　　　0　　　1　　Second DS2 C-bit inverted 　0　　　0　　　1　　　0　　First DS2 C-bit inverted 　0　　　0　　　1　　　1　　Undefined - Do not use 　0　　　1　　　0　　　0　　Third DS2 C-bit &/+ (See Note) DS2 stuff bit inverted 　0　　　1　　　0　　　1　　Second DS2 C-bit &/+ (See Note) DS2 stuff bit inverted 　0　　　1　　　1　　　0　　First DS2 C-bit &/+ (See Note) DS2 stuff bit inverted 　0　　　1　　　1　　　1　　DS2 Stuff bit inverted 　1　　　0　　　0　　　0　　DS2 Stuff bit = 0 　1　　　0　　　0　　　1　　DS2 Stuff bit = 1 　1　　　X　　　1　　　X　　Undefined - Do not use 　1　　　1　　　X　　　X　　Undefined - Do not use Note: & = AND in the transmit direction, + = OR in the receive direction.

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Address	Bit	Symbol	Description
21	7-5	Reserved	**Reserved:** These bits should always be written with a 0.
	4 3 2	R3AIS2 R3AIS1 R3AIS0	**Receive DS3 AIS Selection:** A DS3 AIS may be detected with any one of five different criteria. These three bits select the DS3 AIS detection mechanism that is used for providing an R3AIS alarm, as shown in the table below.

R3AIS2	R3AIS1	R3AIS0	Receive DS3 AIS Selection Criterion
0	0	0	Framed 1010 pattern C-bits = 0 X-bits disregarded
0	0	1	Framed 1010 pattern C-bits = 0 X-bits = 1
0	1	0	Framed 1010 pattern C-bits disregarded X-bits disregarded
0	1	1	Undefined - Do not use
1	0	0	Unframed 1010 pattern
1	0	1	Unframed all ones pattern
1	1	X	Undefined - Do not use

The C-bits = 0 and X bits = 1 conditions are detected as explained for bits 6 and 7 of Address 24H. The other detection conditions are described below.

R3AIS(2-0) set to 000, 001, and 010 respectively:

The framed 1010 pattern detection consists of looking for the 1010 pattern on a per DS3 subframe basis and monitoring for errors in 4-bit groups of the 1010 pattern. The 1010 pattern is accepted as valid if the M13X receives 4 or fewer errored 4-bit groups of the 1010 pattern per DS3 subframe and the 1010 pattern starts with a 1 after each DS3 overhead bit.

R3AIS(2-0) set to 100:

For the unframed 1010 pattern detection the M13X looks for 1010 pattern and declares R3AIS if it receives 2 or fewer errored 4-bit groups of the 1010 pattern per DS3 subframe. The M13X will exit the R3AIS state if it receives 5 or more errored 4-bit groups of the 1010 pattern per DS3 subframe. If 3 - 4 4-bit groups of the 1010 pattern are errored per DS3 subframe the M13X will exit and reenter the R3AIS state.

R3AIS(2-0) set to 101:

The unframed 1111 pattern detection consists of looking for the 1111 pattern and monitoring for errors in 4-bit groups of the 1111 pattern. The 1111 pattern is accepted as valid if the M13X receives 4 or fewer errored 4-bit groups of the 1111 pattern out of a total of 168 4-bit groups.

Address	Bit	Symbol	Description
21 (cont.)	1 0	T3AIS1 T3AIS0	**Transmit DS3 AIS Selection:** A DS3 AIS may be generated in one of four ways. The following table selects the DS3 AIS generation mechanism: T3AIS1 T3AIS0 Transmit DS3 AIS Selection 0 0 ANSI defined AIS generation Note: A 1 must be written to bit 0 of register 01H to set the transmitted DS3 X-bits to 1. 0 1 Framed all ones and C-bits set to 1 1 0 Unframed 1010 pattern 1 1 Unframed all ones pattern Note: These bits must be set to 0 when transmitting DS3 idle (see T3IDL in register 01H).
22	7-0	C1BZn (n=7-0)	**C1 Bit Zero Counter:** A saturating counter that counts the number of C1 bits equal to 0 in both the C-bit parity mode and M13 format mode since the counter was last read. In the M13 format mode the contents of this counter should be disregarded. The counter is inhibited when DS3 loss of signal or out of frame occurs. The counter is cleared when it is read by the microprocessor. When lead $\overline{\text{M13X}}$ is low, this counter is 16 bits wide and this address contains the low byte of that counter. The high byte of the counter is written to the CR register (3EH) when this register is read. When lead $\overline{\text{M13X}}$ is high, this counter is 8 bits wide.
23	7-0	MEn (n=7-0)	**DS3 M-bits in Error Counter:** A saturating counter that counts the number of M-bits that are in error since the counter was last read. The counter is inhibited when DS3 loss of signal or out of frame occurs. The counter is cleared when it is read by the microprocessor. When lead $\overline{\text{M13X}}$ is low, this counter is 16 bits wide and this address contains the low byte of the counter. The high byte of this counter is written to the CR register (3EH) when this register is read. When lead $\overline{\text{M13X}}$ is high, this counter is 8 bits wide.

Address	Bit	Symbol	Description
24	7	AISXEQ1	**DS3 AIS Detection:** This bit provides a filtered indication of the receive DS3 X-bits being equal to 1. Two counters are used to implement this filter, a mod 16 counter CXE1 which counts the receive DS3 X-bit pairs = 11, and a mod 4 counter CXE0 which counts the receive DS3 X-bit pairs = 00. When either counter matures, both counters are reset. The AISXEQ1 bit becomes latched when the CXE1 counter matures. This bit is used for determining if the X-bits = 1 condition is met when R3AIS2 = 0, R3AIS1 = 0, and R3AIS0 = 1 in register 21H (ANSI DS3 defined AIS detection). This is a latched bit, and clears when it is read by the microprocessor. This bit will relatch if the condition that causes this bit to latch is still present.
	6	AISCEQ0	**DS3 AIS Detection:** This bit provides a filtered indication of the receive DS3 C-bits equal to 0. This bit will be set if the M13X receives 7 contiguous DS3 frames with 30 or fewer DS3 C-bits set to 1. This bit is used for determining if the C Bits = 0 condition is met when R3AIS2 = 0, R3AIS1 = 0, and R3AIS0 = X, where X means don't care. This is a latched bit, and clears when it is read by the microprocessor. This bit will relatch if the condition that causes this bit to latch is still present.
	5	Test Bit	**Test Bit:** Used for diagnostic purposes. This bit must always be ignored.
	4	Test Bit	**Test Bit:** Used for diagnostic purposes. This bit must always be ignored.
	3	Test Bit	**Test Bit:** Used for diagnostic purposes. This bit must always be ignored.
	2	Test Bit	**Test Bit:** Used for diagnostic purposes. This bit must always be ignored.
	1	Reserved	**Reserved:** This bit must always be ignored.
	0	SEF	**Severely Errored Frame Indication:** A 1 indicates a Severely Errored Frame (SEF) has been detected. A SEF is defined as 3 out of 16 F-bits are in error, utilizing a sliding window of 16 F-bits. This is a latched bit, and clears when it is read by the microprocessor. This bit will relatch if the condition that causes it to latch is still present.
25	7 6 5 4 3 2 1 0	IRLBALL IRLB25 IRLB21 IRLB17 IRLB13 IRLB9 IRLB5 IRLB1	**Receive Loopback Interrupt Requests:** The bits in these registers are interrupt request bits for the corresponding remote loopback request bits in register 08H. The RISE and FALL bits in register 3FH control whether these interrupt request bits are set on the entrance or exit of an alarm condition, or both. If the corresponding interrupt request mask bit is set to a 1 in register 2EH then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor when a bit in these registers becomes set to 1. A microprocessor read cycle clears all set interrupt request bits in the register that is read.
26	7 6 5 4 3 2 1 0	IRLBDS3 IRLB26 IRLB22 IRLB18 IRLB14 IRLB10 IRLB6 IRLB2	**Receive Loopback Interrupt Requests:** The bits in these registers are interrupt request bits for the corresponding remote loopback request bits in register 09H. The RISE and FALL bits in register 3FH control whether these interrupt request bits are set on the entrance or exit of an alarm condition, or both. If the corresponding interrupt request mask bit is set to a 1 in register 2FH then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor when a bit in these registers becomes set to 1. A microprocessor read cycle clears all set interrupt request bits in the register that is read.

Address	Bit	Symbol	Description
27	7	IRNEW	**New FEAC Message Interrupt Request Bit:** The NEW condition is defined as having received a NEW FEAC message. A NEW FEAC message is understood to have been received when 5 consecutive and identical FEAC messages have been received. The NEW FEAC condition is exited after a NEW FEAC message has been declared. When this bit and its corresponding interrupt request mask bit in register 30H are both set to 1, the INT/$\overline{\text{IRQ}}$ lead is driven active. A microprocessor read cycle clears a set interrupt request bit. The RISE and FALL bits in register 3FH control whether this interrupt request bit is set on the entrance or exit of an alarm condition, or both. Care must be taken by the end user to ensure that the RX FEAC register (1DH) is read within 8.5 ms (16 x 5 DS3 frames or 5 FEAC message times) from the onset of this interrupt request to ensure that the FEAC message that caused this interrupt does not get overwritten with a possible new FEAC message.
	6 5 4 3 2 1 0	IRLB27 IRLB23 IRLB19 IRLB15 IRLB11 IRLB7 IRLB3	**Receive Loopback Interrupt Requests:** The bits in these registers are interrupt request bits for the corresponding remote loopback request bits in register 0AH. The RISE and FALL bits in register 3FH control whether these interrupt request bits are set on the entrance or exit of an alarm condition, or both. If the corresponding interrupt request mask bit is set to a 1 in register 30H then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor when a bit in these registers becomes set to 1. A microprocessor read cycle clears all set interrupt request bits in the register that is read.
28	7	IRSEF	**Severely Errored Frame Interrupt Request Bit:** A severely errored frame is defined as receiving 3 or more DS3 F-bits in error in a sliding window of 16 DS3 F-bits. An SEF defect is terminated when the receive DS3 signal is in frame and there are fewer than 3 DS3 F-bit errors in 16 consecutive F-bits (ANSI T1.231 sec. 7.1.2.2.2). When this bit and its corresponding interrupt request mask bit in register 31H are both set to 1, the INT/$\overline{\text{IRQ}}$ lead is driven active. A microprocessor read cycle clears a set interrupt request bit. The RISE and FALL bits in register 3FH have no effect on the functioning of this interrupt.
	6 5 4 3 2 1 0	IRLB28 IRLB24 IRLB20 IRLB16 IRLB12 IRLB8 IRLB4	**Receive Loopback Interrupt Requests:** The bits in these registers are interrupt request bits for the corresponding remote loopback request bits in register 0BH. The RISE and FALL bits in register 3FH control whether these interrupt request bits are set on the entrance or exit of an alarm condition, or both. If the corresponding interrupt request mask bit is set to a 1 in register 31H then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor when a bit in these registers becomes set to 1. A microprocessor read cycle clears all set interrupt request bits in the register that is read.
29	7 6 5 4 3 2 1 0	IRR3LOS IRR3OOF IRR3AIS IRR3IDL IRR3CKF IRT3CKF $\overline{\text{IRXR2}}$ $\overline{\text{IRXR1}}$	**DS3 Receive Alarms/Status Interrupt Requests:** The bits in this register location are interrupt request bits for the alarm/status bits listed in register location 00H. When a bit in this register and its corresponding interrupt request mask bit in register 32H are both set to 1, the INT/$\overline{\text{IRQ}}$ lead is driven active. A microprocessor read cycle clears a set interrupt request bit. The RISE and FALL bits in register 3FH control whether these interrupt request bits are set on the entrance or exit of an alarm condition, or both.

Address	Bit	Symbol	Description
2A	7 6-0	IRCERROR IRDS2OOFn (n=7-1)	**Latched C-bit Status/DS2 Out Of Frame Interrupt Request Bits:** The bits in this register location are interrupt request bits for the alarm/status bits listed in register location 03H. When a bit in this register and its corresponding interrupt request mask bit in register 33H are both set to 1, the INT/$\overline{\text{IRQ}}$ lead is driven active. A microprocessor read of the register clears all set interrupt request bits. The RISE and FALL bits in register 3FH control whether these interrupt request bits are set on the entrance or exit of an alarm condition, or both.
2B*	7	IRFCSS	**FCS Error Counter Saturated Interrupt Request:** This bit becomes set when the RX FCS Error Counter (3BH) saturates.
	6	IRABTS	**ABORT Counter Saturated Interrupt Request:** This bit becomes set when the RX ABORT Counter (3CH) saturates.
	5	IRFBS	**FEBE Performance/DS3 F-Bit and M-Bit Error Counter Saturated Interrupt Request:** This bit becomes set when the FEBE Performance/DS3 F-bit and M-bit Error Counter (04H) saturates.
	4	IRCPS	**C-Bit Parity Performance/Number of Frames Counter Saturated Interrupt Request:** This bit becomes set when the C-bit Parity Performance/Number of Frames Counter (05H) saturates.
	3	IRPPS	**P-Bit Parity Performance Counter Saturated Interrupt Request:** This bit becomes set when the P-bit Parity Performance Counter (06H) saturates.
	2	IRFMES	**DS3 F-Bits and M-Bits in Error Counter Saturated Interrupt Request:** This bit becomes set when the DS3 F-bits and M-bits in Error Counter (1BH) saturates.
	1	IRC1BZS	**C1 Bit Equal to Zero Counter Saturated Interrupt Request:** This bit becomes set when the C1 Bit Equal to Zero Counter (22H) saturates.
	0	IRMES	**DS3 M-bits in Error Counter Saturated Interrupt Request:** This bit becomes set when the DS3 M-Bits in Error Counter (23H) saturates.

* Note: The bits in register 2BH are latched bits, and they all clear to 0 when it is read by the microprocessor. If a bit and its corresponding interrupt mask bit in register 34H are both set to a 1, then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor. The RISE and FALL bits in register 3FH control whether these interrupt request bits are set on the entrance or exit of an alarm condition, or both.

Address	Bit	Symbol	Description
2C	7-5	IRRHIS2-IRRHIS0	**Receive PMDL Interrupt Request:** The following table lists the various interrupt status indications associated with the receive PMDL message. The significance of these bits is controlled by control bit RHIE (bit 5) in register 3DH.

IRRHIS2	IRRHIS1	IRRHIS0	RHIE	Condition Present
0	0	0	X	Idle condition
0	0	1	X	Start of message indication
0	1	0	0	Valid message received; (FCS checked OK), or the receive FIFO needs servicing (full or overflow).
0	1	0	1	Valid message received; (FCS checked OK), or the receive FIFO needs servicing (half full or more).
0	1	1	X	Message received with FCS error
1	0	0	X	Abort message received
1	1	1	X	Invalid Frame received. (i.e., frame with non-integral number of bytes or with number of bytes (after destuffing) less than 5).
1	0	1	X	Unused Code.
1	1	0	X	Unused code.

These are latched bits that clear when read by the microprocessor. If a bit in this register is set to a 1 and the corresponding interrupt mask bit in register 35H is set to a 1, then the INT/$\overline{IRQ}$ lead goes active to signal an interrupt request to the external microprocessor. Codes of 110 and 101 are not defined. When a condition occurs all three bits are updated at once. For instance, when a start of message occurs, the bits are set to 001, and when an end of message is received the bits will be changed from 001 to 010. The bits are never forced to 000 by the internal logic. They only get set to 000 when a read is performed. The priority for detecting these alarms is:

- Abort (highest)
- Invalid Frame Received
- FCS Error Received
- Start of Message Indication
- Valid Message Received

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Address	Bit	Symbol	Description
2C (cont.)	4-3	IRRXFS1-IRRXFS0	**Receive PMDL FIFO Interrupt Request:** The following table lists the various FIFO status indications associated with the receive PMDL FIFO. <table><tr><th>IRRXFS1</th><th>IRRXFS0</th><th>Condition Present</th></tr><tr><td>0</td><td>0</td><td>Normal. PMDL FIFO less than half full.</td></tr><tr><td>0</td><td>1</td><td>FIFO equal to or more than half full</td></tr><tr><td>1</td><td>0</td><td>FIFO full</td></tr><tr><td>1</td><td>1</td><td>FIFO overflow</td></tr></table> These are latched bits that clear when the register is read by the microprocessor. If a bit in this register is set to a 1 and the corresponding interrupt mask bit in register 35H is set to a 1, then the INT/$\overline{IRQ}$ lead goes active to signal an interrupt request to the external microprocessor. When a condition occurs both bits are updated at once. 00 is never forced by the internal logic. These bits are only set to 00 when a read is performed.
	2-1	IRTXFS1-IRTXFS0	**Transmit PMDL FIFO Interrupt Request:** The following table lists the various FIFO status indications associated with the transmit PMDL FIFO. <table><tr><th>IRTXFS1</th><th>IRTXFS0</th><th>Condition Present</th></tr><tr><td>0</td><td>0</td><td>Normal. PMDL FIFO equal to or more than half full</td></tr><tr><td>0</td><td>1</td><td>FIFO less than half full</td></tr><tr><td>1</td><td>0</td><td>FIFO overflowed (attempt to write to a full FIFO)</td></tr><tr><td>1</td><td>1</td><td>FIFO underflowed. Reported only if EOM is not set when FIFO underflows.</td></tr></table> These are latched bits that clear when the register is read by the microprocessor. If a bit in this register is set to a 1 and the corresponding interrupt mask bit in register 35H is set to a 1, then the INT/$\overline{IRQ}$ lead goes active to signal an interrupt request to the external microprocessor. When a condition occurs both bits are updated at once. 00 is never forced by the internal logic. These bits are only set to 00 when a read is performed.
	0	IRTHIS	**Transmit PMDL Interrupt Request:** A 1 indicates that the transmit PMDL FIFO needs servicing, either because the message is completed, or because the transmit PMDL FIFO transitioned from more than half full to half full, depending on the THIE control bit setting. This is a latched bit, and clears when the register is read by the microprocessor. If this bit is set to a 1 and the corresponding interrupt mask bit in register 35H is set to a 1, then the INT/$\overline{IRQ}$ lead goes active to signal an interrupt request to the external microprocessor.
2D	7-0	Reserved	**Reserved:** These bits are reserved and must always be ignored.

Address	Bit	Symbol	Description
2E	7 6 5 4 3 2 1 0	MIRLBALL MIRLB25 MIRLB21 MIRLB17 MIRLB13 MIRLB9 MIRLB5 MIRLB1	**Receive Loopback Interrupt Request Masks:** If a bit in this register and its corresponding interrupt request bit in register 25H are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
2F	7 6 5 4 3 2 1 0	MIRLBDS3 MIRLB26 MIRLB22 MIRLB18 MIRLB14 MIRLB10 MIRLB6 MIRLB2	**Receive Loopback Interrupt Request Masks:** If a bit in this register and its corresponding interrupt request bit in register 26H are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
30	7	MIRNEW	**New FEAC Message Interrupt Request Mask Bit:** If this bit and its corresponding interrupt request bit in register 27H are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	6 5 4 3 2 1 0	MIRLB27 MIRLB23 MIRLB19 MIRLB15 MIRLB11 MIRLB7 MIRLB3	**Receive Loopback Interrupt Request Masks:** If a bit in this register and its corresponding interrupt request bit in register 27H are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
31	7	MIRSEF	**Severely Errored Frame Interrupt Request Mask Bit:** If this bit and its corresponding interrupt request bit in register 28H are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	6 5 4 3 2 1 0	MIRLB28 MIRLB24 MIRLB20 MIRLB16 MIRLB12 MIRLB8 MIRLB4	**Receive Loopback Interrupt Request Masks:** If a bit in this register and its corresponding interrupt request bit in register 28H are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
32	7 6 5 4 3 2 1 0	MIRR3LOS MIRR3OOF MIRR3AIS MIRR3IDL MIRR3CKF MIRT3CKF MIRXR2 MIRXR1	**DS3 Receive Alarms/Status Interrupt Request Masks:** If a bit in this register and its corresponding interrupt request bit in register 29H are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.

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Address	Bit	Symbol	Description
33	7 6-0	MIRCERROR MIRDS2OOFn (n=7-1)	**Latched C-bit Status/DS2 Out Of Frame Interrupt Request Mask Bits:** If a bit in this register and its corresponding interrupt request bit in register 2AH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
34	7	MIRFCSS	**FCS Error Counter Saturated Interrupt Request Mask:** If this bit and its corresponding interrupt request bit in register 2BH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	6	MIRABTS	**ABORT Counter Saturated Interrupt Request Mask:** If this bit and its corresponding interrupt request bit in register 2BH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	5	MIRFBS	**FEBE Performance/DS3 F-Bit and M-Bit Error Counter Saturated Interrupt Request Mask:** If this bit and its corresponding interrupt request bit in register 2BH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	4	MIRCPS	**C-Bit Parity Performance/Number of Frames Counter Saturated Interrupt Request Mask:** If this bit and its corresponding interrupt request bit in register 2BH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	3	MIRPPS	**P-Bit Parity Performance Counter Saturated Interrupt Request Mask:** If this bit and its corresponding interrupt request bit in register 2BH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	2	MIRFMES	**DS3 F-Bits and M-Bits in Error Counter Saturated Interrupt Request Mask:** If this bit and its corresponding interrupt request bit in register 2BH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	1	MIRC1BZS	**C1 Bit Zero Counter Saturated Interrupt Request Mask:** If this bit and its corresponding interrupt request bit in register 2BH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	0	MIRMES	**DS3 M-bits in Error Counter Saturated Interrupt Request Mask:** If this bit and its corresponding interrupt request bit in register 2BH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
35	7-5	MIRRHIS2- MIRHIS0	**Receive PMDL Interrupt Request Masks:** If a bit and its corresponding interrupt request bit in register 2CH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	4-3	MIRRXFS1- MIRRXFS0	**Receive PMDL FIFO Interrupt Request Masks:** If a bit and its corresponding interrupt request bit in register 2CH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.

Address	Bit	Symbol	Description
35 (cont.)	2-1	MIRTXFS1-MIRTXFS0	**Transmit PMDL FIFO Interrupt Request Masks:** If a bit and its corresponding interrupt request bit in register 2CH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
	0	MIRTHIS	**Transmit PMDL Interrupt Request Mask:** If this bit and its corresponding interrupt request bit in register 2CH are both set to a 1 then the INT/$\overline{\text{IRQ}}$ lead goes active to signal an interrupt request to the external microprocessor.
36	7-0	Reserved	**Reserved:** These bits are reserved and must always be written with 0s.
37	7-0	TX PMDL FIFO	**Transmit PMDL FIFO:** The byte written into this location is written into the transmit PMDL FIFO. Bit 0 corresponds to the first bit transmitted in an HDLC message byte.
38	7-0	RX PMDL FIFO	**Receive PMDL FIFO:** A read cycle for this location transfers one byte from the receive PMDL FIFO to the data bus. Bit 0 corresponds to the first bit received in the HDLC message. At initialization, the receive PMDL FIFO must be cleared by reading this location the number of times indicated by the RX PMDL FIFO DEPTH register (register 3AH) or until the RX PMDL FIFO DEPTH register becomes 0.
39	7-0	RX PMDL MESSAGE LENGTH	**Receive PMDL Message Length:** This register is loaded with the number of bytes in the last received frame if an end of message, abort, invalid frame, or message received with bad FCS event occurs. The microprocessor must read this value before the end of another complete frame is received. This register clears when read. The receive PMDL logic never loads this register with a 0 when a valid PMDL frame is received (this is done so that if a long frame is received, and the receive PMDL message length ends up exceeding 255, and the IRRHIS(2-0) bits get set to 010 to indicate a FIFO fill condition, then it can be known if an end of message was really received.)
3A	7-0	RX PMDL FIFO DEPTH	**HDLC FIFO Depth:** This register indicates the number of data bytes present in the receive PMDL FIFO. The value is in binary. For example, the value 0000 0000 indicates that the FIFO is empty, while a value 0111 1111 indicates that 127 bytes are present. This value is not reset when a new frame is received. The previous frame length is stored in RX PMDL MESSAGE LENGTH, (bits 7- 0) in register 39H, which is updated every time a new complete frame (good or errored) is received. This register value is decreased by microprocessor reads of the RX PMDL FIFO register (register 38H) only. At initialization, this location should read out as 00H. If it does not, repeated reads of the RX PMDL FIFO register should be performed until it does.
3B	7-0	RX FCS ERROR Counter	**RX FCS Error Counter:** A 16-bit saturating counter that counts the number of PMDL messages that contained FCS errors. To read all 16 bits, read this location to get the low byte and then read the common register location (3EH) immediately after to get the high byte. The contents of this counter should be disregarded when M13MODE = 1 or EHR = 0 or lead $\overline{\text{M13X}}$ is high or floating. The counter is inhibited when DS3 loss of signal, out of frame, AIS, or IDLE occurs. The counter is cleared when it is read by the microprocessor. Single counts are not lost during a read cycle. When this counter saturates, an interrupt request bit (IRFCSS) is set in register 2BH.

Address	Bit	Symbol	Description
3C	7-0	RX ABORT Counter	**Receive Abort Counter:** A 16-bit saturating counter that counts the number of abort sequences (1111111) that were detected. To read all 16 bits, read this location to get the low byte and then read the common register location (3EH) immediately after to get the high byte. The contents of this counter should be disregarded when M13MODE = 1 or EHR = 0 or lead $\overline{M13X}$ is high or floating. The counter is inhibited when DS3 loss of signal, out of frame, AIS, or IDLE occurs. The counter is cleared when it is read by the microprocessor. Single counts are not lost during a read cycle. When this counter saturates, an interrupt request bit (IRABTS) is set in register 2BH.
3D	7	DJB	**DJB Control:** When this bit is set to 0, the internal dejitter buffers (DJBs) are bypassed and held in reset. The gapped receive DS1 clock and data are output on the receive DS1 clock and data outputs (CR1-28 and DR1-28). When this bit is set to a 1, the DJBs are taken out of reset and the receive DS1 clock and data are passed through the DJBs before being output on CR1-28 and DR1-28. Also if a local DS1 loopback is enabled via registers 10H-13H and 1EH, while this bit is set to 1, the looped back DS1 data is dejittered.
	6	IPOLAL	**Interrupt Polarity:** The setting of this bit determines the polarity of the INT/$\overline{IRQ}$ lead when that lead is driven active. When this bit is set to a 1, the polarity of the INT/$\overline{IRQ}$ lead is active low. Otherwise, the polarity is active high.
	5	RHIE	**Receive Half Full Interrupt Enable:** This bit controls the IRRHIS(2-0) interrupt request bit logic to allow interrupts to occur for two different FIFO fill conditions in the "010" state. A 1 enables the receive HDLC controller to generate an interrupt when the receive PMDL FIFO is half full or more, or has detected an end of message. When set to 0, the HDLC controller generates an interrupt when a receive PMDL FIFO full or overflow has occurred, or at the end of the message.
	4	EHR	**Enable HDLC Receive Controller:** A 1 enables the HDLC receive controller. After flag detection and zero bit destuffing, the receive bytes from the PMDL C-bits in the C-bit Parity format DS3 frame only are written into a receive FIFO for a microprocessor read access via register 38H (receive PMDL FIFO). A 0 disables the HDLC controller and disables the HDLC receive interrupts.
	3	Reserved	**Reserved:** This bit is reserved and must always be written with a 0.
	2	EOM	**Transmit End Of Message:** A 1 instructs the HDLC controller that the transmit PMDL FIFO contains the last byte in the message. When the FIFO has emptied, the FCS is calculated and transmitted and then this bit is cleared.
	1	THIE	**Transmit Half Full Interrupt Enable:** This bit controls the IRTHIS interrupt request bit logic to allow interrupts to occur at the transmit PMDL FIFO transition from more than half empty to half empty or message complete only. A 1 enables the transmit HDLC controller to generate an interrupt when the transmit PMDL FIFO transitions from more than half empty to half empty or has detected an end of message. When set to 0, the HDLC controller generates an interrupt only at the end of the message, or when a FIFO underflow has occurred.

Address	Bit	Symbol	Description
3D (cont.)	0	EHT	**Enable HDLC Transmit Controller:** A 1 enables the Transmit PMDL controller. The PMDL C-bits in the transmit DS3 frame are derived from the transmit PMDL controller. The transmitter will send flags when the transmit PMDL FIFO is empty. The bytes are formatted into a message when the transmit PMDL FIFO has bytes present, which is done by loading the TX PMDL FIFO register (register 37H) repeatedly with the byte content of the message to be sent. At the end of the message, a FCS is calculated and transmitted. A 0 disables the transmit PMDL controller, clears the transmit PMDL FIFO, and disables the PMDL transmit interrupts. In this case, the PMDL C-bits in the transmit DS3 Frame are derived from the external transmit C-bit interface (M13MODE = 0) or from the internal stuffing logic (M13MODE = 1).
3E	7-0	CR	**Common Register for High Byte of 16-Bit Counters:** When the low byte of a 16-bit counter is read, its high byte is simultaneously written to this register and preserved for later access. In this way, the high byte and low byte values correspond to the same instant in time.
3F	7-2	Reserved	**Reserved:** These bits are reserved and must always be written with a 0.
	1	RISE	**Rising Edge Sets Interrupt Request Bits:** This control bit works in conjunction with the FALL control bit (described below) for controlling the alarm status bit transition used for setting the interrupt request bits. RISE=1 causes setting of the interrupt request bits on the 0 to 1 transition of the alarm. Register 2CH is not affected by the setting of this bit. The interrupt request bits in register 2CH are always set on the rising edge of the alarm condition. **RISE / FALL / Action** 0 / 0 / The appropriate interrupt request bits are disabled from being set. 0 / 1 / The appropriate interrupt request bits become set when an alarm/condition is removed. 1 / 0 / The appropriate interrupt request bits become set when an alarm/condition is entered. 1 / 1 / The appropriate interrupt request bits become set when an alarm/condition is either entered or removed.
	0	FALL	**Falling Edge Sets Interrupt Request Bits:** This control bit works in conjunction with the RISE control bit (described above) for controlling the alarm status bit transition used for setting the interrupt request bits. FALL=1 causes setting of the interrupt request bits on the 1 to 0 transition of the alarm. Register 2CH is not affected by the setting of this bit. The interrupt request bits in register 2CH are always set on the rising edge of the alarm condition.

APPLICATION DIAGRAM

A typical Channelized T3 application is shown below.
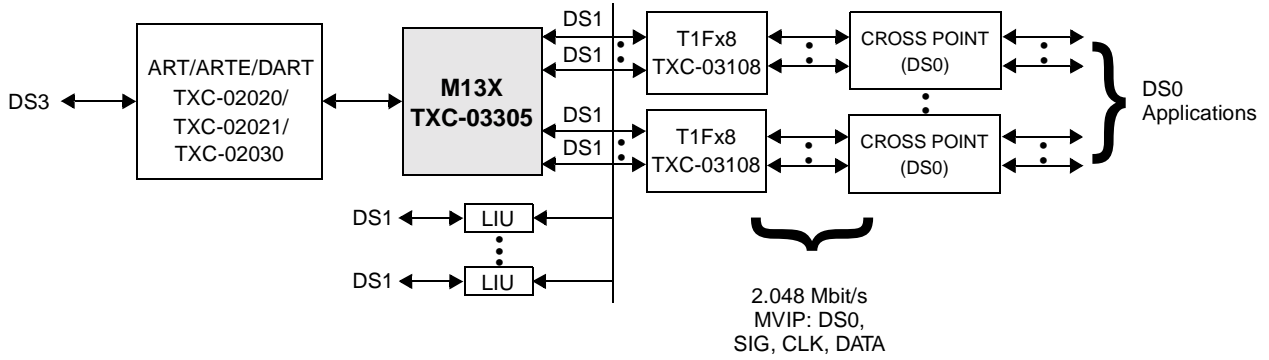
Figure 26. Example Channelized T3 Application

Transswitch has a "Channelized T3 Reference Design" Technical Manual, document number TXC-21114-TM1, available for use with this device. It may be viewed or printed from the "Products/M13X" page of the Transwitch Wold Wide Web Site (www.transwitch.com).

PACKAGE INFORMATION

The M13X device is available in two package formats. A 208-lead small outline plastic ball grid array package suitable for surface mounting is illustrated in Figure 27. A 208-lead plastic quad flat package, suitable for surface mounting, is shown in Figure 28.

.
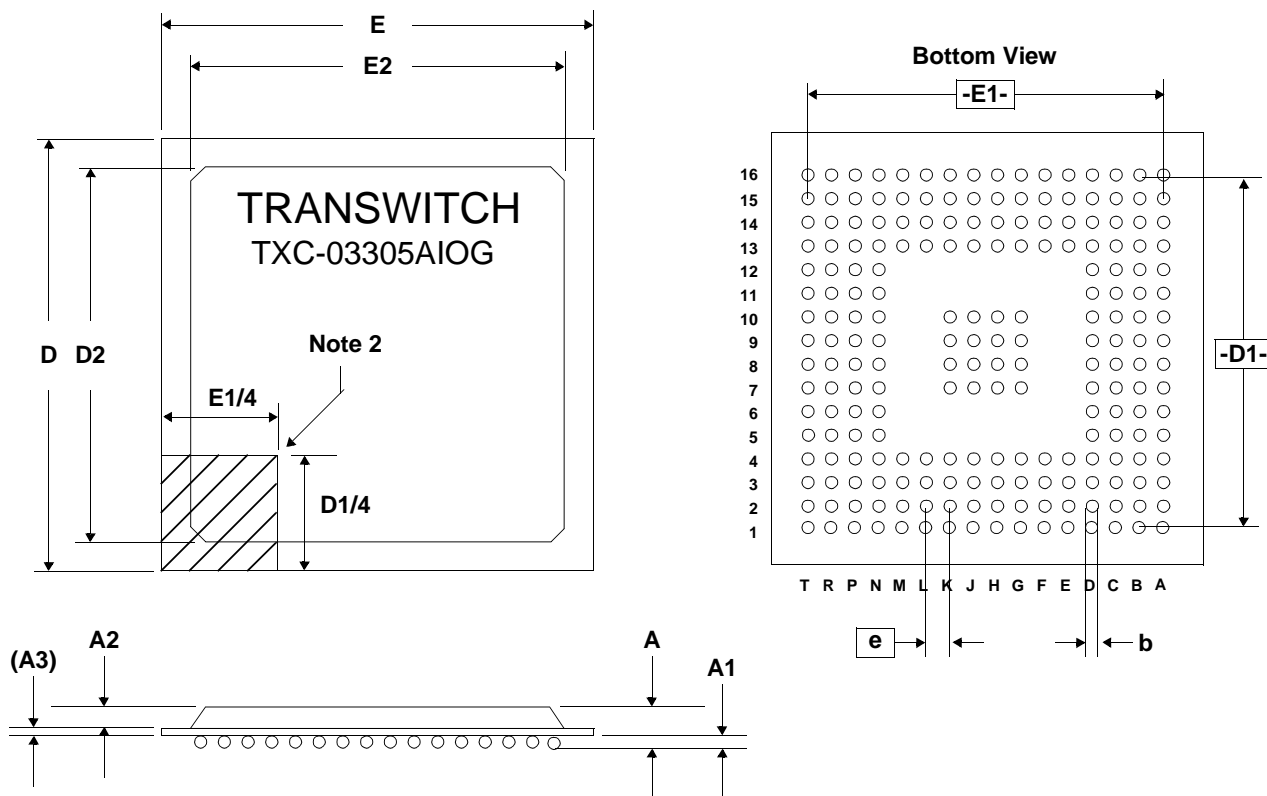
Notes:

1. All dimensions are in millimeters. Values shown are for reference only.

2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.

3. Size of array: 16 x 16, JEDEC code MO-151/B-AAE-1

Dimension (Note 1)	Min	Max
A	1.35	1.75
A1	0.30	0.50
A2	0.75	0.85
A3 (Ref.)	0.36	
b	0.40	0.60
D	17.00	
D1 (BSC)	15.00	
D2	15.00	15.70
E	17.00	
E1 (BSC)	15.00	
E2	15.00	15.70
e (BSC)	1.00	

Figure 27. M13X TXC-03305 208-Lead Plastic Ball Grid Array Package

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TXC-03305AIPQ

See Details "B" and "C"

0.50 typ

Detail "B"

0.17 (MIN)
0.27 (MAX)

Detail "C"

LEAD #1
INDEX

25.50 SQ

28.00 ± 0.10 SQ

30.60 ± 0.25 SQ

SEE DETAIL "A"

4.07 (MAX)

0.25 (MIN)

3.20
3.60

0.09
0.20

0° -7°

0.60 +0.15
-0.10

DETAIL "A"

Note: All dimensions shown are in millimeters and are nominal unless otherwise indicated.
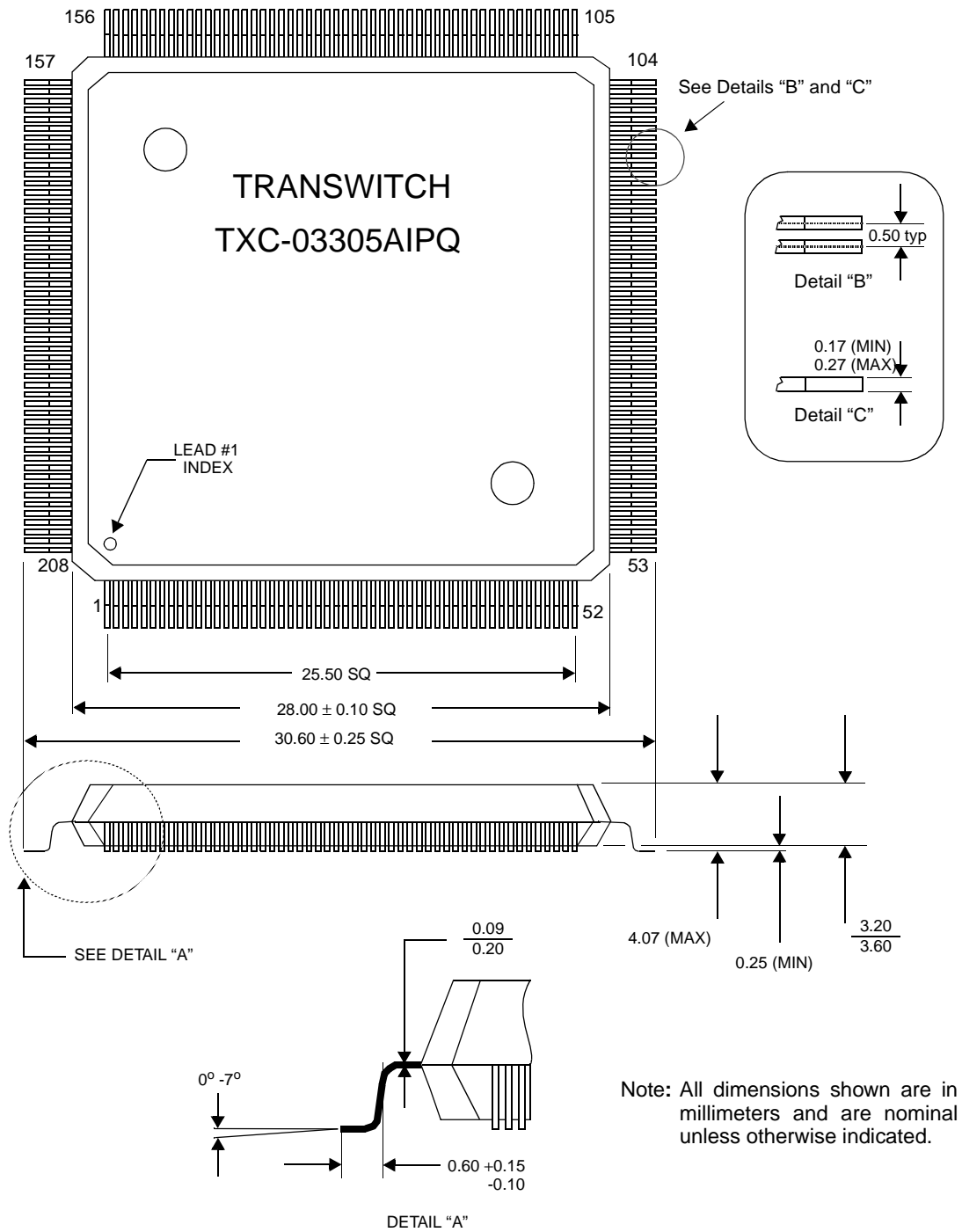
Figure 28. M13X TXC-03305 208-Lead Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-03305AIOG   208-lead Small Outline Plastic Ball Grid Array Package.

Part Number: TXC-03305AIPQ   208-lead Plastic Quad Flat Package.

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ART performs the transmit and receive line interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02021, ARTE VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ARTE has the same functionality as ART, plus extended features.

TXC-02030, DART VLSI Device (Advanced E3/DS3 Receiver/Transmitter). DART performs the transmit and receive line interface functions required for transmission of E3 (34.368 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-20153G, DS3/STS-1 Line Interface Module (DS3LIM-SN). Complete and compact analog-to-digital interface that converts B3ZS-encoded DS3 or STS-1 line signals to and from NRZ data and clock signals. Packaged as 2.6 inch x 1.0 inch 50-lead DIP.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). This is a dual-mode device, which can be configured either to emulate the TXC-03001 device or to provide additional capabilities.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This is a dual-mode device, which can be configured either to emulate the TXC-03003 device or to provide additional capabilities.

TXC-03011, SOT-1E VLSI Device (SONET STS-1 Overhead Terminator). This device provides extended features relative to the 84-lead TXC-03001 and TXC-03001B SOT-1 devices, and it has a 144-lead package.

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). A 4-channel framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. It has extended features relative to the QDS1F device. Requires +5.0 V power supply.

TXC-03108, T1Fx8 VLSI Device (8-Channel T1 Framer). An 8-channel framer for voice and data communications applications. This device handles all logical interfacing functionality to a T1 line and operates from a power supply of 3.3 volts.

TXC-03452B L3M VLSI Device (Level 3 Mapper/Desynchronizer) - L3M maps a DS3 or E3 signal into an SDH/SONET signal formatted for STM-n (VC-3 via TU-3) or STS-n (via STS-1 SPE).

TXC-04201B, DS1MX7 VLSI Device (DS1 Mapper 7-Channel). Maps seven 1.544 Mbit/s DS1 signals into any seven selected asynchronous or byte-synchronous mode VT1.5 or TU-11 virtual tributaries carried in a SONET or SDH synchronous payload envelope.

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TXC-04251, QT1M VLSI Device (Quad DS1 to VT1.5 or TU-11 Async Mapper-Desync). Interconnects four DS1 signals with any four asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface.

TXC-05150, CDB VLSI Device (Cell Delineation Block). Provides cell delineation for ATM cells carried in a physical line at rates of 1.544 to 155 Mbit/s.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device provides features similar to those of the TXC-03011 SOT-1E device, but it operates from a power supply of 3.3 volts rather than 5 volts.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations

ANSI (U.S.A.):

American National Standards Institute	Tel: (212) 642-4900
11 West 42nd Street	Fax: (212) 302-1286
New York, New York 10036	Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real	Tel: (650) 949-6700
Suite 304	Fax: (650) 949-6705
Mountain View, CA 94040	Web: www.atmforum.com

ATM Forum Europe Office

Av. De Tervueren 402	Tel: 2 761 66 77
1150 Brussels	Fax: 2 761 66 79
Belgium	

ATM Forum Asia-Pacific Office

Hamamatsu-cho Suzuki Building 3F	Tel: 3 3438 3694
1-2-11, Hamamatsu-cho, Minato-ku	Fax: 3 3438 3698
Tokyo 105-0013, Japan	

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association	Tel: (800) 854-7179 (within U.S.A.)
Global Engineering Documents	Tel: (314) 726-0444 (outside U.S.A.)
7730 Carondelet Avenue, Suite 407	Fax: (314) 726-6418
Clayton, MO 63105-3329	Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute	Tel: 4 92 94 42 22
650 route des Lucioles	Fax: 4 92 94 43 33
06921 Sophia Antipolis Cedex	Web: www.etsi.org
France	

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (508) 650-1375
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5111
Fax: 22 733 7256
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97124

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 693-6232 (outside U.S.A.)
Fax: (503) 693-8344
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: (800) 521-CORE (within U.S.A.)
Tel: (908) 699-5800 (outside U.S.A.)
Fax: (908) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsu-cho Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated M13X Data Sheet that have significant differences relative to the previous and now superseded M13X Data Sheet:
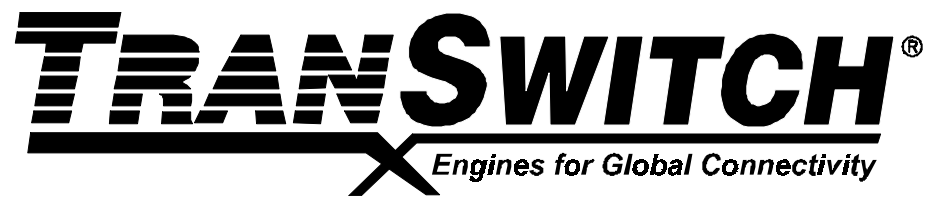
Updated M13X Data Sheet: Ed. 4, September 2000

Previous M13X Data Sheet: *PRELIMINARY* Ed. 3, April 2000

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
All	Removed all *"PRELIMINARY"* indications from document.
2-3	Changed Table of Contents and List of Figures.
23	Added last row to the Absolute Maximum Ratings and Environmental Limitations table that states the LATCH-UP specification.
95	Added reference to the Channelized T3 Reference Design in the Applications Section.
98	Changed reference to TXC-20153D in Related Products section to TXC-20153G.
100 -101	Changed Standards Documentation Sources section.
102	Changed List of Data Sheet Changes Section.

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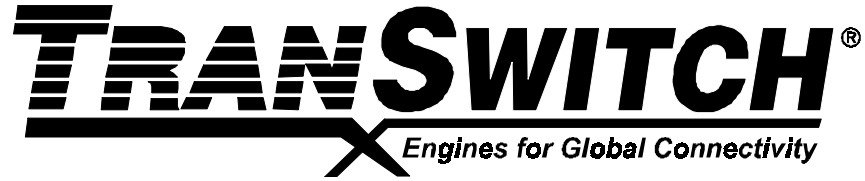
TXC-03305-MB
Ed. 4, September 2000

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